Design and Analysis of SiGe Millimeter-Wave Radio Front-End MMICs For 5G Communication

Raju Ahamed

School of Electrical Engineering

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Thesis supervisor:

Prof. Kari Halonen

Thesis advisors:

M.Sc. Dristy Parveg

D.Sc. (Tech.) Mikko Varonen

Aalto University
School of Electrical
Engineering

AALTO UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING

ABSTRACT OF THE
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Author: Raju Ahamed

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Supervisor: Prof. Kari Halonen

Advisors: M.Sc. Dristy Parveg, D.Sc. (Tech.) Mikko Varonen

This thesis focuses on design and realization of millimeter-wave radio front-end circuits for fifth generation(5G) wireless communication in 0.13um silicon-germanium(SiGe) BiCMOS process. Radio front-end includes single-pole double-through (SPDT) switch, low noise amplifier (LNA) and buffer amplifier(BA) as a part of radio frequency(RF) transceiver system for E-band. The SPDT switch utilizes the reveres saturated SiGe heterojunction bipolar transistor(HBT). The resulting reverse saturated switch shows an insertion loss of 1 dB , isolation of 26 dB, reflection coefficient better than 25 dB at 75 GHz and provides a bandwidth of 40 GHz. A single to differential ended low noise amplifier(LNA)is designed using transformer balun. Simultaneous noise and impedance matching is used in order to realize both low noise and low reflection at the same time. The post layout simulation of E-band low noise amplifier exhibits a gain and noise figure(NF) of 26 dB and 5.5 dB respectively with a power consumption of 33.5 mW. The buffer amplifier shows a gain of 5.5 dB at 75 GHz. Finally, the receiver achieved a gain of 19.6 dB, noise figure(NF) of 6.9 dB and impedance matching better than 13.5 dB at 75 GHz. A 3 dB bandwidth of more than 12 GHz is achieved from the receiver. Extensive simulation results showing the performance of each circuit of receiver are presented.

Keywords: Millimeter-wave, SiGe, BiCMOS, Reverse-Saturation, SPDT, Low noise amplifier, Transformer balun, MMIC

Preface

This thesis was carried out from September 2016 to June 2017 at Aalto University, in collaboration with VTT technical research centre of Finland Ltd. My experience and interest in Millimeter-Wave Integrated Circuits led me to choose this topic as my thesis.
I would like to thank my supervisor, Professor Kari Halonen for giving me the opportunity to work on this thesis and his excellent guidance and support toward this research.
I would like to express my sincere gratitude to my advisors, Dristy Parveg and Dr. Mikko Varonen, for motivating, helping and guiding me in proper way through-out the thesis work. Without their support and guidance I would never have been able to finish this work successfully.
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Raju Ahamed

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Symbols and abbreviations

Symbols

B	Stability measure
BW	Bandwidth
C_S	Center for the input section gain circle
C_L	Center for the output section gain circle
C_F	Center for the noise circle
C_{be}	Base-to-emitter capacitor
C_{bc}	Base-to-collector capacitor
f_{max}	Maximum frequency of oscillation
f_T	Unity current gain frequency
F	Noise factor
F_{cas}	Total noise factor in cascaded system
G	Power gain
G_S	Real part of source admittance
I_{REF}	Reference current
ICP_{1dB}	Input 1-dB compression point
$IP3$	Third-order intercept point
K	Stability factor
L_{stub}	Shunt stub
NF_{min}	Minimum noise figure
OCP_{1dB}	Output 1-dB compression point
P_{DC}	DC power consumption
Q	Quality factor
R_S	Radius for the input section gain circle
R_L	Radius for the output section gain circle
R_F	Radius for the noise circle
R_N	Equivalent noise resistance
R_b	Base resistance
R_{on}	On-resistance of the shunt device
R_{off}	Off-resistance of the shunt device
R_{eq}	Equivalent resistance
S_{11}	Input match
S_{22}	Output match
SNR_{in}	Signal-to-noise ratio at the input
SNR_{out}	Signal-to-noise ratio at the output
V_{dd}	Supply voltage
Y_S	Source admittance
Y_{opt}	Optimum admittance
Z_L	Load impedance
Z_S	Source impedance
Γ_S	Source reflection coefficient
Γ_L	Load reflection coefficient
Γ_{IN}	Input reflection coefficient
Γ_{OUT}	Output reflection coefficient
λ	Wavelength

Abbreviations

AC	Alternating Current
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BJT	Bipolar Junction Transistor
CE	Common Emitter
CMOS	Complementary Metal-Oxide-Semiconductor
CAD	Computer-aided Design
CPW	Coplanar Waveguide
DC	Direct Current
ESD	Electrostatic Discharge
EM	Electromagnetic
FET	Field-Effect Transistor
GaN	Gallium Nitride
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IF	Intermediate Frequency
IoT	Internet of Things
InP	Indium Phosphide
LNA	Low-Noise Amplifier
LO	Local Oscillator
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
nFET	Negative channel Field-Effect Transistor
PA	Power Amplifier
RF	Radio Frequency
SiGe	Silicon-Germanium
SPDT	Single-Pole Double-Throw
SPST	Single-Pole Single-Throw
VM	Vector Modulator
5G	Fifth-Generation
4G	Fourth-Generation

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1 Introduction

1.1 5G Communication

Currently, the Fourth Generation(4G) wireless communication system is being used in different countries. Despite all the technological advances made in the evaluation of 4G, there are still some challenges such as latency, data rate and bandwidth that cannot be accommodated to the existing communication system [1]-[2]. In addition, the number of users is increasing dramatically who need faster internet access to communicate with others or to access information [1]. In recent years, video-conferencing, online gaming, e-health and e-education have been introduced to rapidly growing global subscribers [2]. Furthermore, it has been anticipated by the Wireless World Research Forum (WWRF) that 7 billion people will be served by 7 trillion wireless devices by 2017 [3]. Because of the increased number of wireless mobile devices and services, the demand for higher data rate and lower latency is increasing rapidly. Therefore, a new generation of wireless technology is required to meet the modern demands.

5G will stand as a solution to overcome the limitations of current systems. 5G is the abbreviated form of the fifth generation wireless communication system. The future 5G focuses on higher data speed, lower latency, less energy consumption and more bandwidth [4]. Higher bandwidth allows lower data price. Low latency is a crucial factor in case of self-driven cars because the cars need to communicate with each other and make decision quickly [5]. 5G is expected to be deployed beyond 2020 [4].

5G will be beneficial for all group of people including but not limited to students and professionals. Right now, the 4G is always in the context of mobile phones. 5G will not only be used in mobile phones but also in lots of wirelessly connected devices [1]-[4]. It will be the foundation of autonomous driving, virtual reality office and Internet of Things (IoT) [4]-[5]. A doctor can easily treat a patient sitting in the remote part of the globe by the help of this faster technology [7]. A student can attend his class sitting in any part of world. The world will be advanced further by taking the advantages of a faster network. Rapid improvement in the performance will be noticed in different sectors like education, transportation, healthcare, manufacturing, media and entertainment [6]. Therefore, 5G is considered the greatest revolution in the era of technology.

Millimeter-Waves (30 GHz to 300 GHz) are considered as the key frequency candidates for the future 5G communication as it can offer very high data rate in broadband mobile and backhaul service [8]. The International Tele-communication Union (ITU)has released the E-bands frequencies 71–76 GHz and 81–86 GHz to provide broadband wireless services which is widest radio spectrum available today [9]. Due to the low atmospheric attenuation this band makes it suitable for millimeter-wave transmissions [2]. Therefore, E-band stands as an attractive choice in the next generation wireless communication.

1.2 Beam Forming Transceiver

The path loss between transmit and receive antennas is given as in [10]

$$\frac{P_{RX}}{P_{TX}} = G_{RX} G_{TX} \frac{\lambda^2}{4\pi} \frac{1}{4\pi R^2} \tag{1}$$

where P_{RX} is received power, P_{TX} is transmit power, G_{RX} is the gain of receive antenna, G_{TX} is the gain of transmit antenna and R is the distance between transmitter and receiver. This equation is known as Friss transmission equation. From this equation it can be seen that the path loss is inversely proportional to the square of the wavelength. The smaller the wavelength, the higher the path loss. Therefore, at millimeter wavelengths the path loss is extremely high. In order to overcome this strong attenuation, beam steering techniques can be used at mm-wave frequencies [11]-[12]. Beam-steering technique increases the received signal strength and provide large spatial coverage [11]-[12].

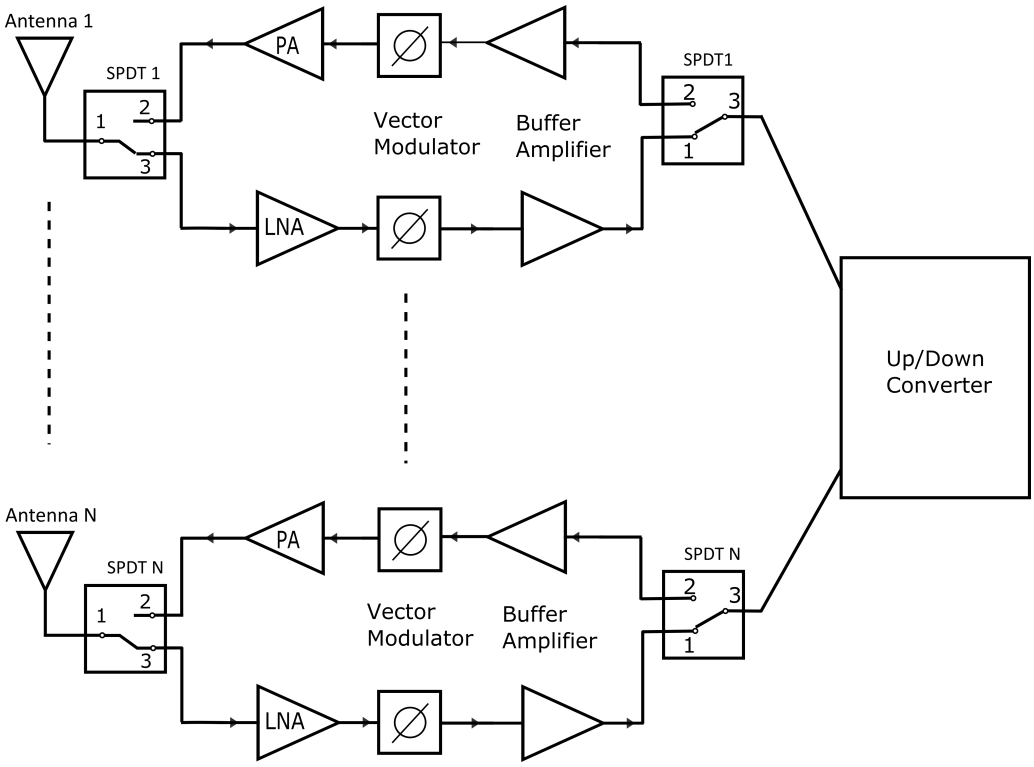


Figure 1.1: Simplified Block Diagram of a Beam Forming RF Transceivers

This targeted 5G communication system will be executed with the beam forming transceivers. Figure 1.1 shows the simplified block diagram of RF beam forming transceiver system. The system consists of many components. The first element after the antenna is single-pole double-through (SPDT) switch. In this approach, a single antenna is shared by both transmitter and receiver using this front end SPDT switch. The receiver path comprises of low noise amplifier (LNA), vector modulator (VM),

buffer amplifier and down-converter. The transmitter path consists of up-converter, buffer amplifier, vector modulator and power amplifier(PA). The low noise amplifier provides significant gain so that the total noise figure in the receiver is determined by the low noise amplifier. The vector modulator is used to serve the purpose of beam-steering by changing the phase. Buffer amplifiers provide additional gain in both transmitter and receiver chain. The up-conversion mixer converts the base-band signal to the carrier signal in the transmitter. The down-conversion mixer is used in the receiver to convert the high frequency incoming signal to base-band signal for further processing.

1.3 SiGe Technology for Millimeter-Wave Applications

At present, several process technologies are available such as III-V(GaAs,GaN), SiGe/BiCMOS and CMOS. An important question comes to the mind of millimeter-wave designers: what IC technology to use for millimeter-wave applications. Generally, the millimeter-wave field has been dominated by III-V semiconductor technologies [13]. Even though they present superior performance, they have low yield and limited integration capability.

CMOS IC technology offers higher levels of integration and reduced cost when produced in large volume compared to III-V semiconductor process [14]. However, at millimeter-wave frequency it suffers from some serious limitations. Currently, SiGe technology shows superior RF performance over CMOS in terms of common performance metrics such as f_{max}, f_T and breakdown voltage [15]. As reported in [16], 130nm SiGe already achieved f_T and f_{max} of 300 GHz and 500 GHz respectively. Consequently, SiGe HBT based technologies have gained increasing interest for emerging millimeter-wave application domain. In case of CMOS technology, it is difficult to relate the f_T of the naked device to final circuit performance. On the otherhand, the relation between performance metrics f_T, f_{max}, fcross and circuit performance is well understood in SiGe technology [17]. Additionally, bipolar transistors are less sensitive to interconnect parasitics due to a higher trans-conductance and favourable transistor terminal impedances for a given power consumption [15]. Therefore, SiGe will remain the best candidate as semiconductor technology in millimeter-wave applications.

1.4 SiGe Heterojunction Bipolar Transistors

A regular bipolar homojunction transistor uses same material in both of the p-type and n-type region. On the other hand, a heterojunction bipolar transistor uses different materials for p-type and n-type regions. The heterojunction bipolar transistor contains silicon n-type region and silicon-germanium (SiGe) p-type region [18]. The resultant device consists of silicon n-type emitter, silicon-germanium (SiGe) p-type base and silicon n-type collector. Therefore, both of the base-emitter and base-collector junctions are heterojunctions. Due to this fact, they are called heterojunction bipolar transistor (HBT).

SiGe HBT is the first practical bandgap engineered transistor in silicon material system [13]. SiGe HBT offers significant benefits. First of all, it provides higher f_T making it suitable for high frequency applications compared to normal BJT [19]. Secondly, SiGe HBT can be easily adapted to silicon CMOS to form monolithic SiGe HBT BiCMOS technology [18]. Typical SiGe HBT BiCMOS processes have 20% additional mask count compared to normal CMOS processes. This increases 20% additional manufacturing step and cost which is acceptable compromise between performance and cost [18].

1.5 Goal of This Thesis

This work focuses on the design of millimeter-wave beam forming transceiver on a single chip at E-band. In particular, the circuits are single-pole double-through (SPDT) switch, low noise amplifier (LNA) and buffer amplifier as a part of beam forming transceiver system.

1.6 Thesis Organization

Chapter 1 provides a brief overview of 5G communication and system architecture. Design of millimeter-wave single-pole double-through (SPDT) switch has been presented in chapter 2. Results has been shown and analyzed to evaluate the performance of designed switch. In chapter 3, detailed design of millimeter-wave low noise amplifier has been presented. Simulation results have been also presented to analyze and evaluate the designed E-band low noise amplifier. Design of buffer amplifier has been presented in chapter 4 with simulation results. In chapter 5, the performance of the whole receiver has been analyzed. Finally, main results of each circuit and the overall receiver performance have been summarized and evaluated in chapter 6.

2 Millimeter-Wave Switch Design

2.1 Transmit-Receive Switch

In many applications front-end switches are often used so that both the transmitter and receiver can share the same antenna. Millimeter wave switches are used in communication system for switched beam antennas, multi-band receiver on chip, built-in-Self-Test(BIST) circuits and instrumentation systems [20]-[21]. Using a single antenna for both the transmitter and receiver increases integration and reduces array size which in turn reduces the cost. Switch is a critical component in the transceiver because the performance of switch has great effect on the transceiver's performance. In the transmit mode, the switch loss directly reduces the output power of the transmitter. In the receive mode, the switch loss directly contributes to the overall noise figure of the system as the switch loss is added to the signal before any amplification. Figure 2.1 shows the basic front-end transmit-receive switch. The switch connects the antenna to the transmitting path or receiving path. During transmission period, the antenna is connected to the transmitter. Similarly, the antenna is connected to the receiver during the receive mode.

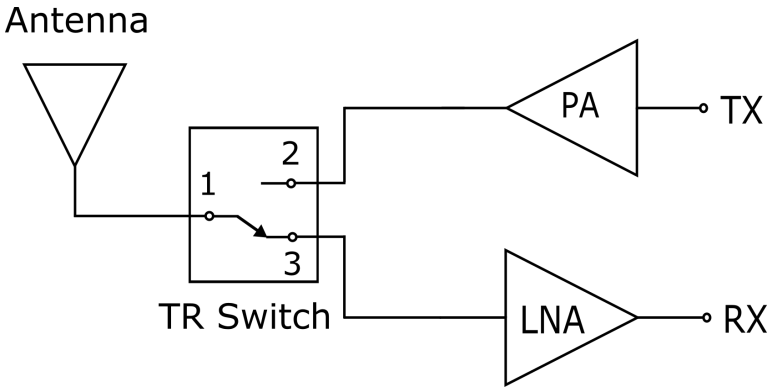


Figure 2.1: Front-end switch being used to share the same antenna by both transmitter and receiver

RF switches can be implemented in any of the technologies like CMOS, III-V and SiGe. CMOS swithces offer low cost and reduced power consumption. For superior performance, an expensive III-V techonology can be used [22]- [23]. In [24], it has been reported that a SiGe heterojunction bipolar transistor(HBT) can be used to improve the performance of switches and their performance is comparable to the performance of expensive III-V technology. Although there are a variety of technologies employed in RF switches, SiGe HBT is chosen in this work due to its improved performance. This work presents the design of high performance SPDT switch using saturated SiGe HBT.

2.2 Performance Metrics of RF Switch

In general, every RF device is characterized by a set of voltage wave ratios called "S-parameters". The transmission through a path or reflection from a port of the device can be characterized by S-parameters. In case of RF switch, most important performance metrics are insertion loss, isolation and reflection coefficient. Most significant S-parameters of a single-pole double-through(SPDT) are shown in Figure 2.2. In this figure, S_{21}, S_{31} and S_{11} represent the insertion loss, isolation and reflection coefficient for the SPDT switch respectively.

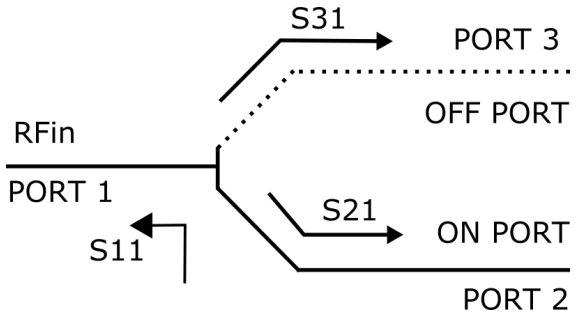


Figure 2.2: Significant S-parameters of SPDT switch

S_{21} represents the forward voltage gain. In case of most switches and other passive devices, it represents the insertion loss. Insertion loss should be as low as possible to make the switch efficient.

Isolation is another important switch parameter. Assuming the SPDT switch as a three-port network where port 2 is ON and port 3 is OFF, this is the parameter which determine how much power is wasted due to leakage through the off arm. It is determined from the transmission coefficient S_{31}. A high isolation switch is often desired to reduce the leakage.

The input reflection coefficient is represented by S_{11}. It is defined as the voltage ratio of the reflected wave on the input port to the original incident wave. It can be used to determine the return loss. The return loss represents the power loss from impedance mismatches. A low reflection coefficient is desired to ensure that all of the power is transmitted through the switch.

There are some other parameters which are also equally important. One of them is power handling capability. Power handling capability plays an important role in switch design. The switch must handle the output power from the power amplifier if the switch is used in a transceiver application. This property is measured by input referred 1 dB compression point($P1dB$). The higher the value of $P1dB$, the larger power a switch can handle without degrading the switching performance. In addition, the third order intercept point ($IP3$) is a measure of the degradation of signal quality in a device. It represents how strong is the third order intermodulation product. Another important parameter is switching speed. The Switching speed is the ability to switch rapidly. The switching speed can affect the data rate.

2.3 Millimeter-Wave Switch Topology

There exists a wide variety of switch topologies. Three major topologies are series, shunt and series-shunt. Most of the switches employ series-shunt topologies at microwave frequencies. However, at millimeter-wave frequencies, using series device becomes difficult because they add loss during the on-state and suffer from capacitive feed-through during the off-state [25]. As a result, shunt transistors are typically used in millimeter-wave switch design. The most commonly used topology for millimeter-wave switch is quarter-wave shunt switch topology [20]-[21].

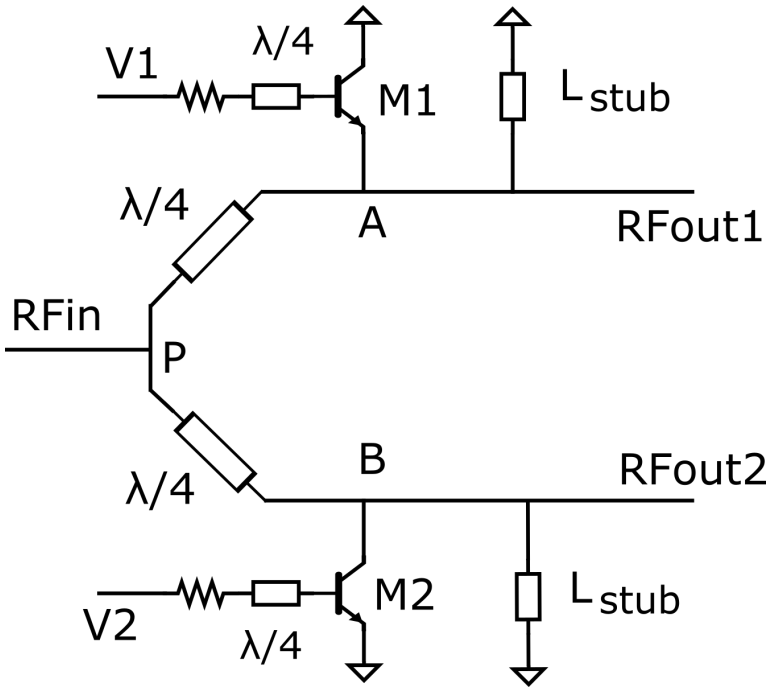


Figure 2.3: Schematic of quarter-wave shunt SPDT switch using SiGe HBT

Figure 2.3 shows the quarter-wave shunt switch using SiGe HBT. In this topology, the upper device M1 is turned on with a high voltage at V1 and there is a low impedance at point A. The quarter-wave transmission line transform the low impedance at point A into an approximately open circuit at the junction point P. Therefore, the upper-half of the switch presents nearly open circuit. As a results, RF energy at junction point P is blocked from traveling towards the RF_{out1}. On the other-hand, the lower device M2 is turned off with a zero voltage at V2 and there is an approximate open circuit at point B. Therefore, a low loss path is created between RF_{in} port and RF_{out2} port which allows most of the RF energy to flow towards the RF_{out2} port. Figure 2.4 shows the working principle of a quarter-wave shunt SPDT switch in a clear and simple way. When the device will be in the on-state by high voltage at the base, the corresponding arm will be in nonconducting mode and vice versa.

A shunt transmission line L_{stub} is used to resonate with the capacitance of the shunt device at the desired frequency. The shunt stub also provide the DC ground reference

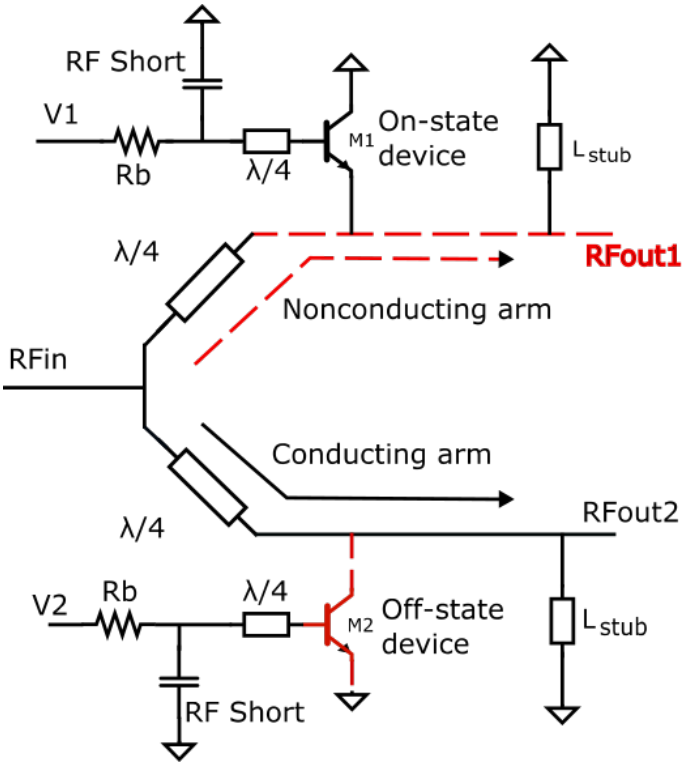


Figure 2.4: Working principle of quarter-wave shunt SPDT switch using SiGe HBT

to the transistor terminal. As the capacitance of a shunt device is resonated out with L_{stub}, the performance of the switch is determined by the equivalent on-resistance(R_{on}) and off-resistance(R_{off}) of the shunt device. The insertion loss depends on (R_{off}). It is determined by how large resistance the off-sate shunt device can present. Isolation is determined by how small resistance(R_{on}) the on-state shunt device can present. Therefore, a larger R_{off} can provide lower insertion loss and smaller R_{on} can provide higher isolation. There is a quarter-wave transmission line at the base of transistor. The other terminal of transmission line is connected to the RF short circuiting capacitor. The quarter-wave bias line presents a large impedance at E band and low impedance at lower frequencies. The task of this quarter-wave line is to provide isolation from base to ground at the E band.

2.4 Analysis of Shunt HBT Device

The shunt HBT can be analyzed using the small signal model of the device. Figure 2.5 shows the small signal model of the shunt SiGe HBT where R_{bc} is the diffusion resistance from the base to collector junction and C_{bc} represents the junction and diffusion capacitance from the base to collector. R_{be} and C_{be} represent the resistance and capacitance of the base-emitter junction. C_s is the collector to substrate capacitance and R_s is the substrate resistance. The equivalent resistance and capacitance are given in (1) and (2) according to [18] where $R_{be} \approx R_{bc}$

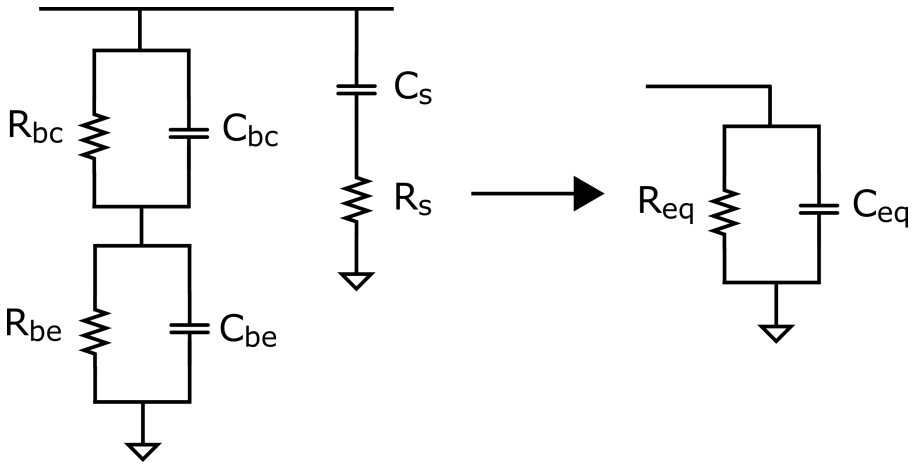


Figure 2.5: Small signal model of the shunt SiGe HBT

$$R_{eq} = \frac{2R_{be}[1 + (\omega R_s C_s)^2]}{1 + (\omega R_s C_s)^2[1 + \frac{2R_{be}}{R_s}]} \tag{2}$$

$$C_{eq} = \frac{C_{be}}{2} + \frac{C_s}{(1 + \omega R_s C_s)^2}. \tag{3}$$

When the switch is conducting, the shunt device in the corresponding arm is in the off-state and vice versa. As the off-sate capacitance is resonated out with the shunt stub L_{stub}, the equivalent off-state resistance determine the performance of the off-state shunt HBT. In the off-state, $R_{be} \gg R_s$ and the equivalent off-state resistance R_{eq-off} is given by

$$R_{eq-off} = R_s + \frac{1}{\omega^2 R_s C_s^2}. \tag{4}$$

In the on-state, $R_{be} \ll R_s$ and the equivalent on-state resistance R_{eq-on} is given by

$$R_{eq-on} = 2R_{be}. \tag{5}$$

The on-state capacitance can be ignored as the corresponding switch arm will not conduct.

2.5 Design of Saturated Quarter-Wave Shunt SPDT Switch

Whenever a designer starts to work on the switch design, several critical questions come to mind. The designer needs to think about the sizing of device for optimum performance. Matching network is another main concern for the designer. To design and optimize quickly, a methodology was proposed in[16]. The approach is beneficial to save time for iteration and it can provide intuitive insight into design tradeoffs. Saturation of HBT represents a biasing condition when both of the junctions in the device are forward biased. This section explain the design of forward saturated quarter-wave shunt SPDT switch.

2.5.1 Choosing the device size

Choosing the optimal device size appears as a primary challenge in design of quarter-wave shunt switch. The performance for different device sizes can be compared and an optimal size can be selected. To do this job, it takes a large number of iterations and the inductive stub needs to resonate with the device capacitance for each size. But, the method described below can reduce the the iteration greatly. First, it is assumed that device capacitance will be resonated out for each size. In this case, R_{eq-on} and R_{eq-off} can be extracted from the Y parameter of the shunt device. Now, using the value of R_{eq-on} and R_{eq-off} and equations (6) to (10) derived in [18], insertion loss and isolation can be plotted.

$$R_{p-up} = \frac{Z_0^2}{R_{eq-on}//Z_0} \tag{6}$$

$$R_{p-down} = \frac{Z_0^2}{R_{eq-off}//Z_0} \tag{7}$$

$$\Gamma = \frac{R_{p-up}//R_{p-down} - Z_0}{R_{p-up}//R_{p-down} + Z_0} \tag{8}$$

$$IL = \sqrt{(1-\Gamma^2)(\frac{R_{p-up}}{R_{p-up}+R_{p-down}})(\frac{R_{eq-off}}{R_{eq-off}+Z_0})} \tag{9}$$

$$Isolation = \sqrt{(1-\Gamma^2)(\frac{R_{p-down}}{R_{p-up}+R_{p-down}})(\frac{R_{eq-on}}{R_{eq-on}+Z_0})} \tag{10}$$

Figure 2.6 shows the plot of R_{eq-on} and R_{eq-off} of forward saturated device for various value of multipliers at the frequency of 75 GHz. The multiplier represents the number of transistor in parallel. The unit emitter width is 900 nm. It is known that the wider the device, the smaller the resistance will be. From the figure it can be seen that as the number of multiplier increases, both the on and off resistance of shunt device decreases as expected. Smaller R_{on} provides higher isolation. So, the device with a higher multiplier provides better isolation. On the other hand, a smaller R_{off} provides higher insertion loss. As a result, the device with a higher multiplier suffers from higher insertion loss. As a result, there is always trade-off between isolation and insertion loss. Therefore, the device size should be chosen carefully in order to achieve the required insertion loss and isolation.

Figure 2.7 shows the calculated insertion gain and isolation of forward saturated SPDT switch for different values of multiplier. The figure agrees well to the theory. It is interesting to note that, when the multiplier is too small (e.g.less than 5), the isolation is significantly low. This is due to the fact that, the device shows high impedance although it is in ON state for a smaller multiplier. It should be noted that during the calculation of insertion gain and isolation, the loss of quarter of transmission line was neglected. However, this calculation provides excellent approximation to choose the device size for optimum performance. Therefore, the device with a multiplier of 30 was chosen to have a moderate isolation and low insertion loss. The final emitter area of the device is 30x(0.07 um)x(0.9 um).

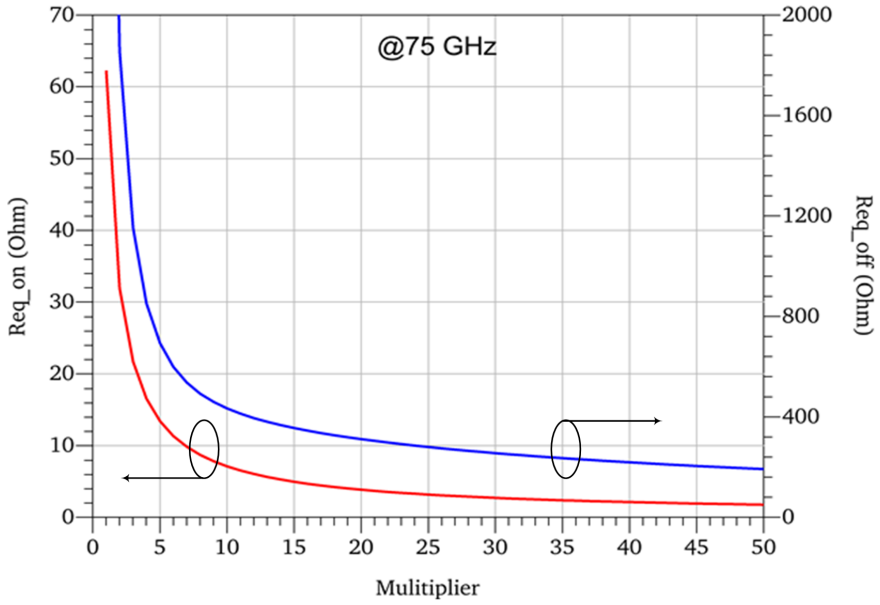


Figure 2.6: Equivalent on and off resistance of the forward saturated shunt HBT for different values of multiplier

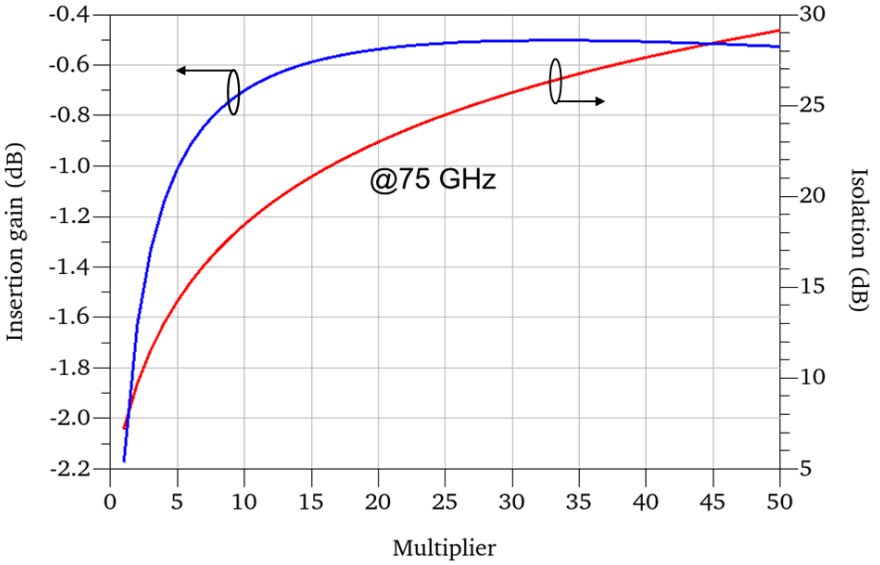


Figure 2.7: Calculated insertion gain and isolation of forward saturated shunt SPDT switch

2.5.2 Designing matching network

Device size has already been chosen with a great care. The next important step for the switch is to design the impedance matching network. Matching network has great impact on the performance and it determines the operating frequency of the switch. As discussed previously, the parasitic capacitance dominates the bandwidth

performance. So, to remove the effect of this capacitance it should be resonated out by some means. Inductive shunt stub has been used to resonate out the parasitic capacitance. For nFET device on- and off-state capacitance are nearly equal. But in case of bipolar device on-state capacitance and off-state capacitance differs. Figure 2.8 shows the on and off-state capacitance of SiGe HBT. It is clear that the capacitance are different from each other and off state capacitance has higher value than the on state capacitance. The stub is designed to resonate the off-state capacitance out as the device in the conducting arm is in the off state. So, this capacitance is resonated out to have low reflection coefficient at the desired frequency. This shunt stub was realized by a microstrip transmission line. The on-state capacitance is not important as the corresponding arm is in nonconducting state.

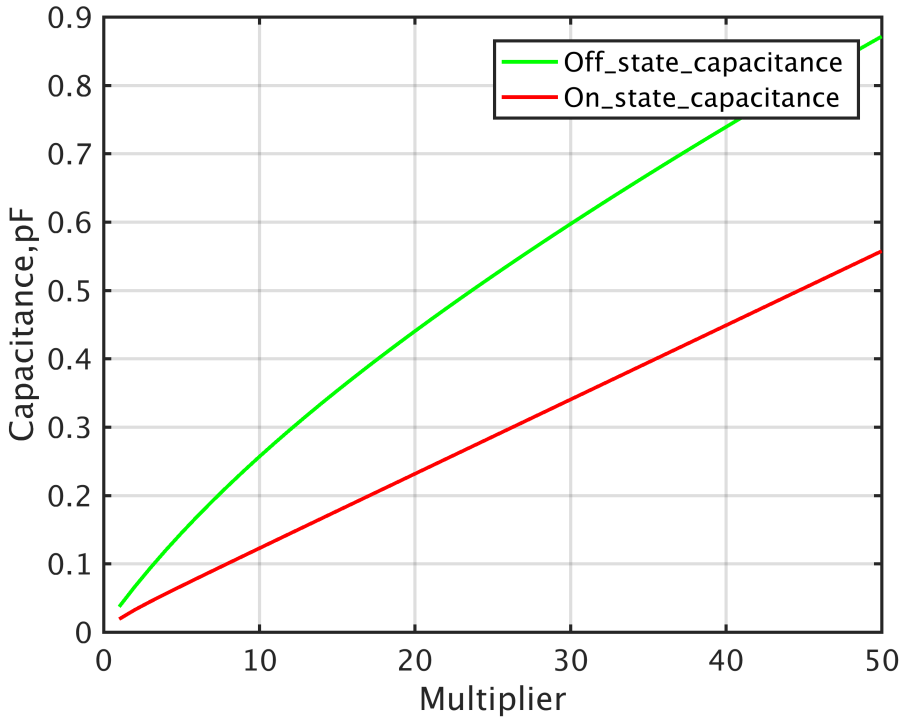


Figure 2.8: On and off state parasitic capacitance of SiGe HBT

2.6 Reverse-Saturated Shunt SPDT switch

The SiGe HBT in Figure 2.4 can be flipped so that the collector is connected to ground and the emitter is connected to RF signal path. The new configuration is called the reverse saturated HBT. The schematic of shunt switch using reverse saturated HBT is shown in Figure 2.9.

There is a significant reason behind using this reverse saturation topology. The reason is improved insertion loss compared to the forward saturation topology [25]. Figure 2.10 presents the reason for improvement in insertion loss using reverse saturated

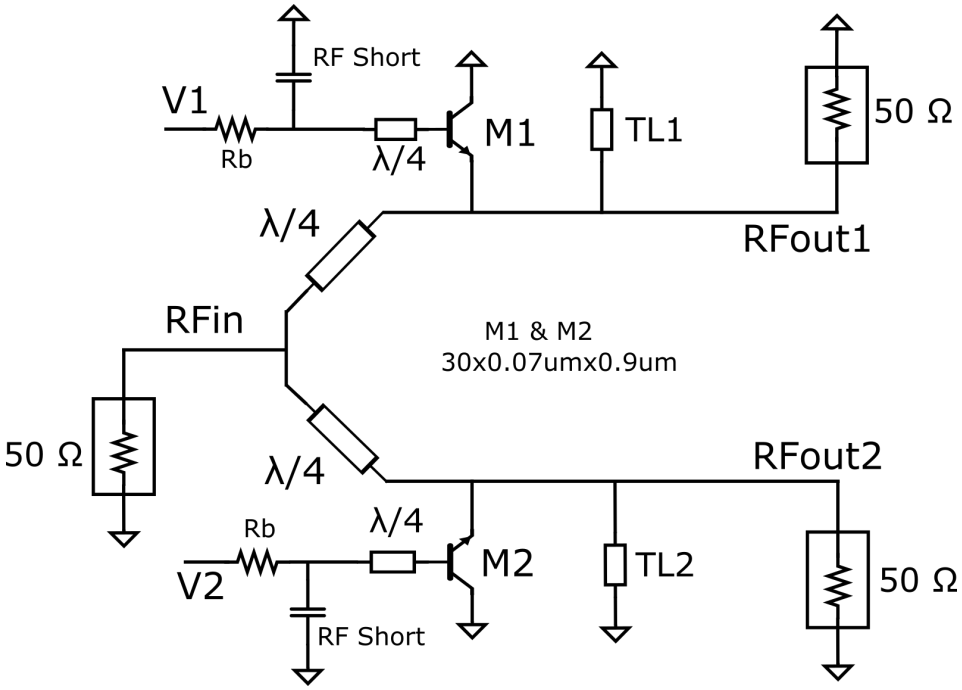


Figure 2.9: Schematic of the reverse-saturated shunt SPDT switch

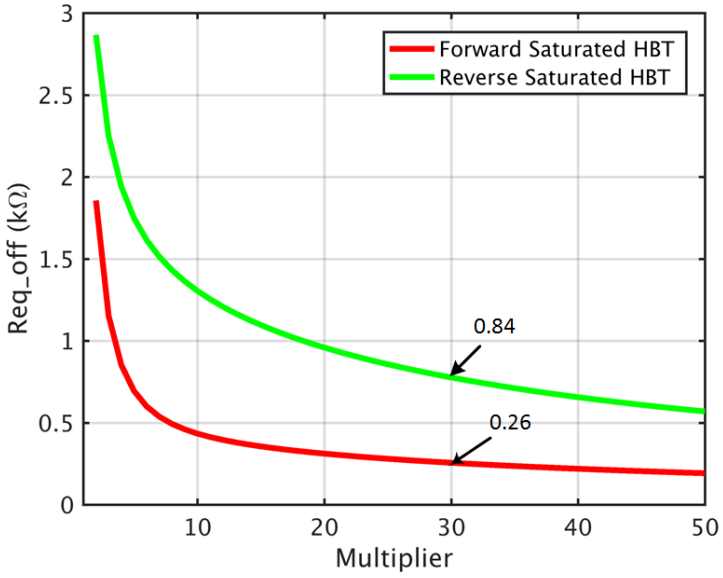


Figure 2.10: Off-resistance of forward and reverse saturated SiGe HBT

HBT. This figure shows the off-resistance for both forward-saturated HBT and reverse-saturated HBT for various number of multiplier. The simulation frequency is at 75 GHz according to the goal of this thesis. It clearly shows that the equivalent off-resistance for the reverse-saturated device is significantly higher than that of the forward-saturated device. For example, when the number of multiplier is 30, equivalent off-resistance (Req_off) for forward saturated HBT is 840 Ω whereas it

is only 260 Ω for the reverse saturated HBT.

$$FoM = \frac{R_{eq-on}}{R_{eq-off}} \tag{11}$$

$$FoM_{reverse} = \frac{840}{3} = 280 \tag{12}$$

$$FoM_{forward} = \frac{260}{3} = 87 \tag{13}$$

$$FoM_{reverse} = 3.21 FoM_{forward} \tag{14}$$

Equations (10)-(13) show that the figure of merit(FoM) for the reverse saturated case is 3.21 times higher than the forward saturation. The improvement in equivalent off resistance is mainly due to higher emitter doping and also due to better isolation of emitter from the Si substrate [26].

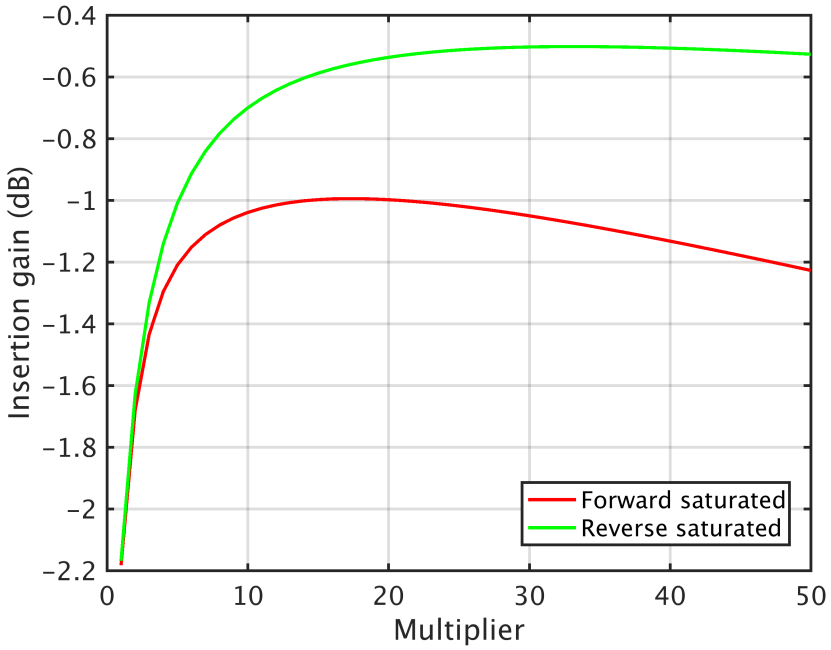


Figure 2.11: Calculated insertion gain of forward and reverse saturated shunt switch

Figure 2.11 shows the calculated insertion gain for both of the forward and the reverse saturation cases. For a multiplier of 30, the insertion loss in the forward saturated switch is 0.65 dB higher than in the reverse saturated switch. However, on state equivalent resistance shows same values for both of the topology. As a result, the calculated isolation is almost same for both of the forward and reverse saturation case. Calculated isolation for both of the topology is shown in Figure 2.12. As the insertion loss remains constant when device multiplier exceeds 20 and isolation

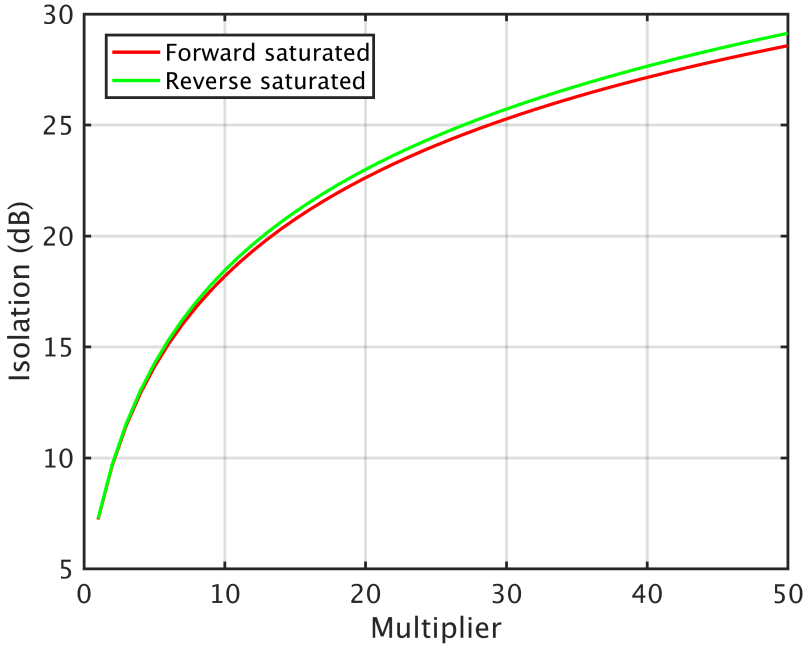


Figure 2.12: Calculated isolation of forward and reverse saturated shunt switch

continues increasing, a larger large multiplier has been chosen for higher isolation and lower insertion loss. The final multiplier value has been chosen to be 30. The emitter area of the device again became 30 µm × 0.07 µm x 0.9 µm. Therefore, for both of the cases the value of multiplier value has been selected to be 30 which will make it easier to compare the performance. In a switch a high value of current flows through the base. The bias resistance Rb is used to limit the bias current flowing through the base. The value of Rb is 30 Ω. Performance of both forward saturated and reverse saturated switches are shown and analyzed in the next section.

2.7 Performance Analysis of SPDT Switch

Performance of quarter-wave shunt SPDT switches with both forward and reveres saturated HBT will be analyzed here. Each port of both switches is terminated to 50 Ω. Same device size has been chosen for both of configurations. The number of multiplier was 30 and the emitter area was 30x (0.07 um)x(0.9 um) for each device. As the off- state capacitance is different for forward and reverse saturated HBT, the length of transmission line was also of different value. A length of 304 µm and 230 µm has been utilized to resonate out the capacitance for reverse and forward topology respectively.

2.7.1 Insertion loss

The insertion gain of quarter-wave shunt SPDT switches with both forward and reverse saturated HBTs is shown in Figure 2.13. The reverse saturated switch provides 1 dB of insertion loss at 75 GHz and less than 1.5 dB of insertion loss within the

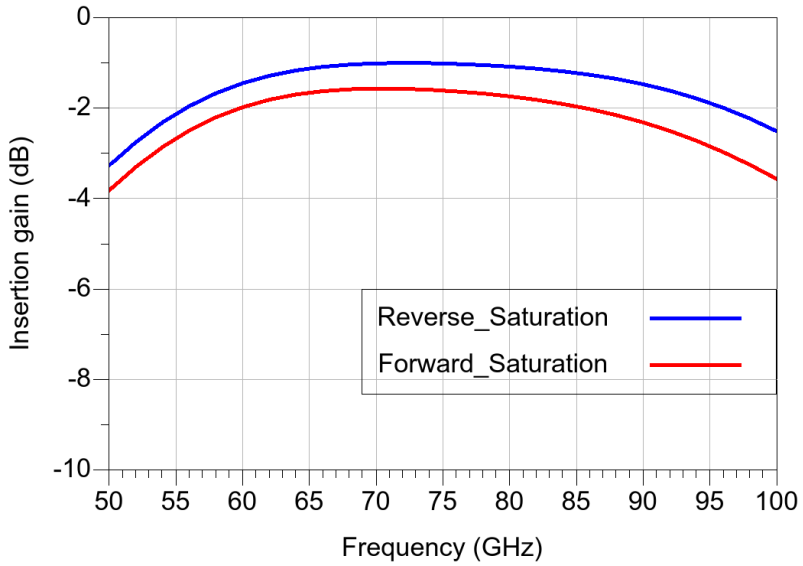


Figure 2.13: Simulated insertion gain of forward and reverse saturated shunt switch

whole E band (60-90 GHz). The calculated insertion was 0.5 dB at 75 GHz. The additional loss comes from the transmission lines. On the other hand, a switch with forward saturated HBTs provides 1.6 dB of insertion loss at the center frequency 75 GHz and less than 2.3 dB for whole E band. So, there is clear improvement in insertion loss in reverse saturation topology which was anticipated in the early stage of design. Moreover, both of the topologies offer significantly wide bandwidth performance.

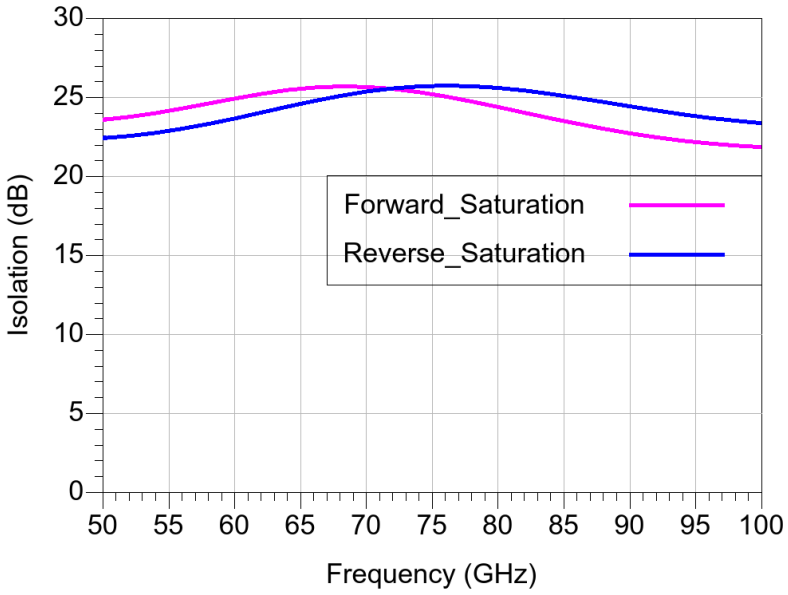


Figure 2.14: Simulated isolation of forward and reverse saturated shunt switch

2.7.2 Isolation

From the calculated result of isolation, it has been shown that both of the topologies have the same isolation. The value of the anticipated isolation was better than 25 dB for both of forward and reveres saturated switch. Figure 2.14 shows the simulation result of isolation for both of the topologies. The simulated values agree well to the calculated values and provides better than 25 dB of isolation. The minimum isolation is better than 22.7 dB from 60 to 90 GHz for both of the switch configurations. Isolation shows significantly wide-band response. Even higher isolation than current switch could be achieved by selecting the larger device. But larger device would consume more power and cause higher insertion loss. So, if higher isolation is needed, larger device size can be used sacrificing insertion loss and consuming more DC power.

2.7.3 Reflection coefficient

The simulated reflection coefficient for both the forward and reverse saturated shunt switches are shown in Figure 2.15. The input return loss for reverse saturated switch is more than 40 dB at the center frequency and better than 12 dB for the whole E band. The switch with forward saturated HBTs achieved a input return loss of 24 dB at 75 GHz and better than 11 dB through-out the E band. Similarly, simulation results provide greater than 10 dB of output matching for the both of topologies from 60 GHz to 90 GHz. The goal of this thesis was to achieve a 30 GHz bandwidth from 60 GHz to 90 GHz. Therefore, bandwidth requirement has been fulfilled from the quarter-wave SPDT switch.

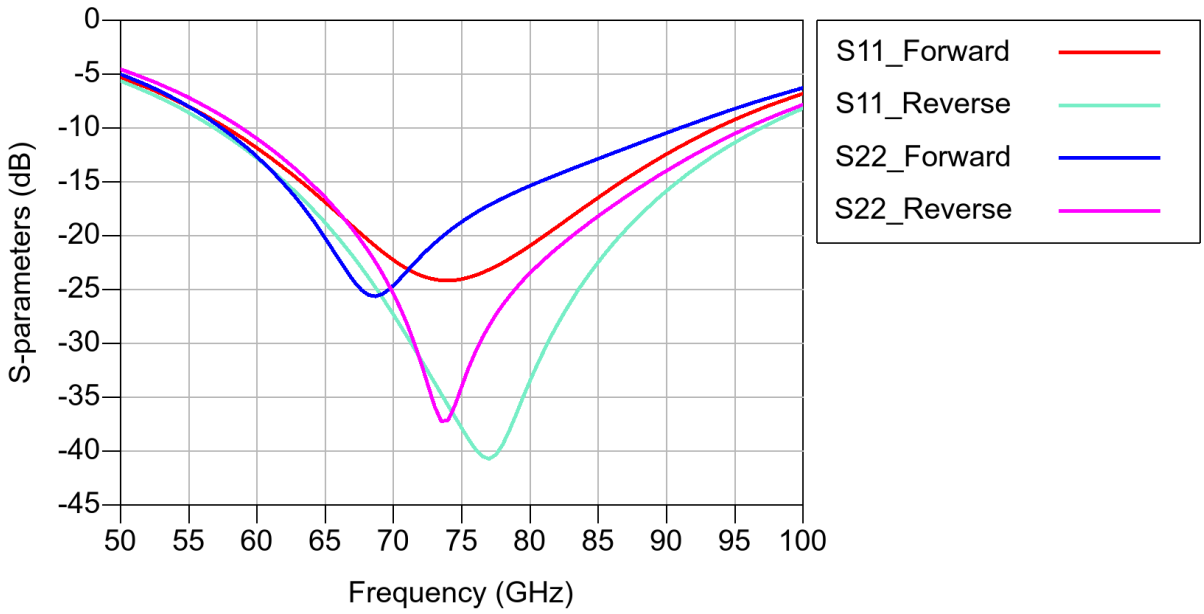


Figure 2.15: Simulated impedance matching of forward and reverse saturated shunt switch

2.7.4 Noise figure

In the receive mode, the switch noise figure directly contributes to the overall noise figure of the system as the switch noise is added before any amplification. The noise figure of passive device is nearly same as the insertion loss. Figure 2.16 shows the noise figure of forward and reverse saturated shunt switch. As expected, the noise figure is 1.6 dB at 75 GHz for the forward case and 1 dB for the reverse saturated case.

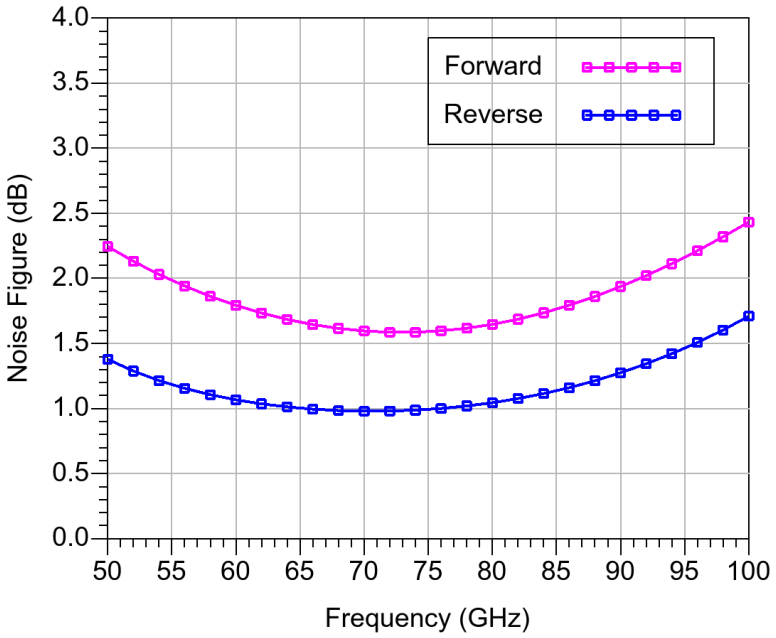


Figure 2.16: Simulated noise figure of forward and reverse saturated shunt switch

2.7.5 Power handling

If the switch is used in transceiver to change the path between transmitter to receiver, the switch must have high power handling capability. Because, the switch needs to be able to handle the high power from the power amplifier of the transmitter path. However, the semiconductor switches suffer from the limited power handling capability. The key reason behind the limited power handling capability comes from the fact that a significant amount of voltage appears at the base of an off state device. The source of this base voltage is the parasitic capacitance of the device. This parasitic capacitance appears as a result of pn-junction from base to collector and base to emitter of the Bipolar device.

The effect of parasitic capacitance when the power amplifier(PA) is transmitting power to the antenna is shown in Figure 2.17. C_{bc} and C_{be} represent the parasitic capacitance of the bipolar transistor. C_{bc} is is the base to collector capacitance and C_{be} is the base to emitter capacitance. Due to parasitic capacitance, voltage at switch port is capacitively divided to base node. If the power from the PA is very high, there

will be significant voltage at the base node to turn on the transistor. As a result of turning on the transistor, power will leak through the transistor. Therefore,the power handling capability of shunt switch is highly dependent on the turn on voltage of the transistor. The higher the turn on voltage of the transistor, the higher power handling capability the switch has. As the SiGe HBT has larger turn on voltage compared to a FET device, the SiGe based design has better power handling capability than the FET based design.

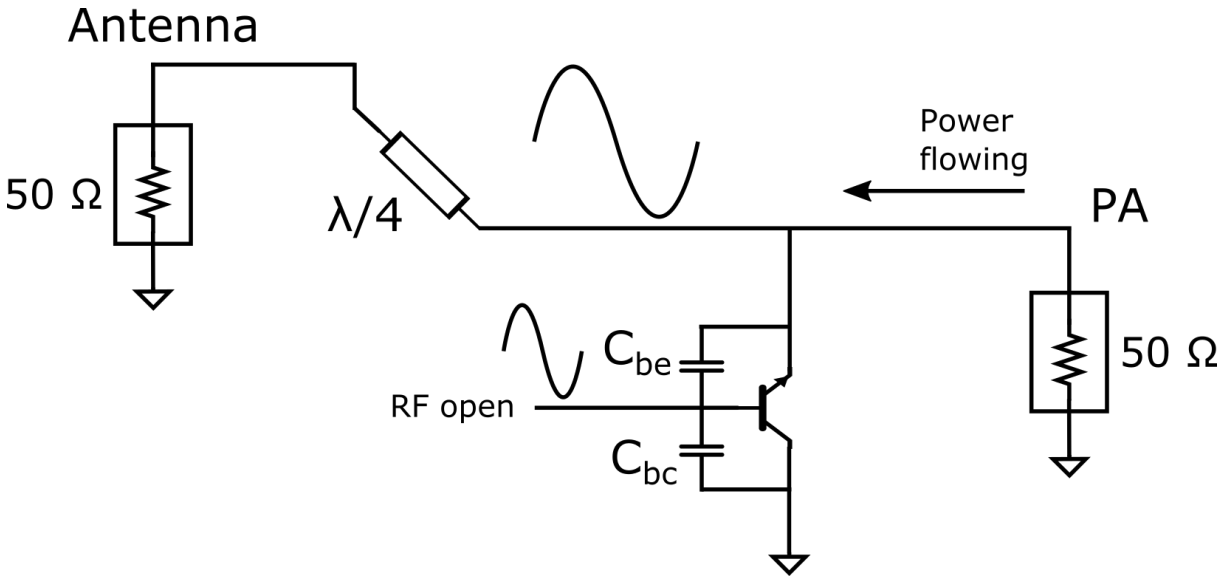


Figure 2.17: Effect of parasitic capacitance on power handling capability

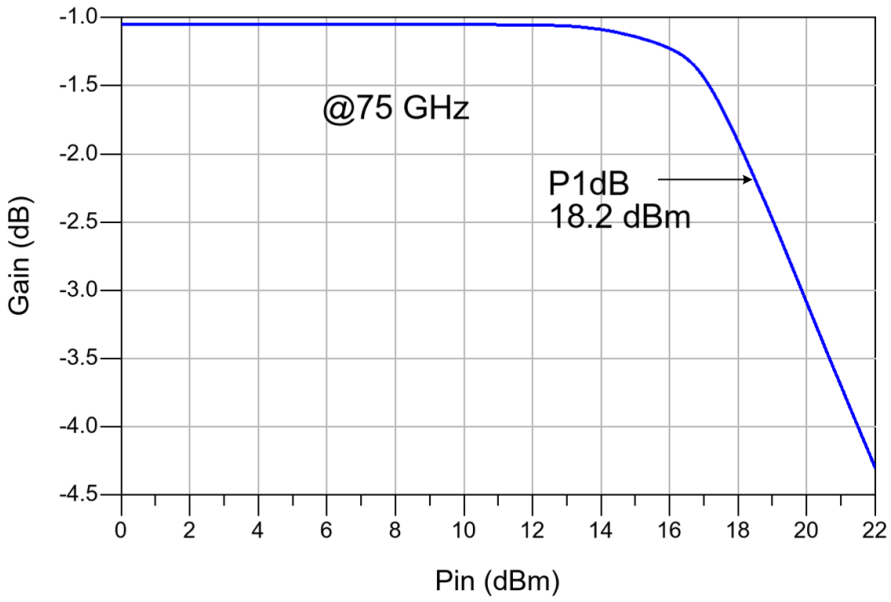


Figure 2.18: Simulated 1 dB compression point of reverse saturated shunt SPDT switch

Power handling capacity of a circuit is represented by 1 dB compression point (P1dB). Figure 2.18 shows the 1 dB compression point of the reverse saturated SPDT switch. The simulated value of P1dB is 18.2 dBm. As C_{bc} and C_{be} are almost same for the bipolar transistor, the power handling ability of both forward saturated and reverse saturated switch will be nearly equal.

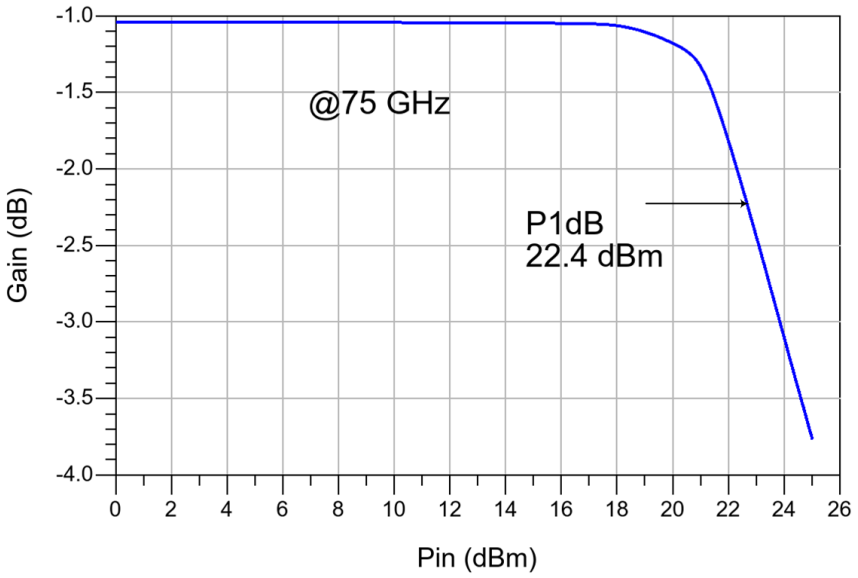


Figure 2.19: Simulated 1 dB compression point of reverse saturated shunt SPDT switch with a negative bias voltage

In order to handle even more power, different techniques might be applied. Applying negative bias can be one of the techniques. If a negative dc supply is applied to the base of the transistor , P1dB should increase. This is possible due to the fact that off state impedance remain same if a negative DC voltage is supplied at base but it takes a larger RF swing at the switch port to reach a turn on voltage of the transistor. Figure 2.19 shows the simulated 1 dB compression point of reverse saturated shunt SPDT switch with a negative bias voltage. The magnitude of this negative voltage is 0.5 V. However, this technique needs further investigation to confirm the validity. Because, although collector-base voltage (Vbc) remain below the breakdown voltage, base-emitter voltage (Vbe) exceeded the process limitation.

PIN diode can be used in a SPDT switch to handle more power. In [27] a P1dB of +24 dBm has been achieved using PIN diode in 90 nm SiGe process. According to [28], a P1dB of +24 dBm has been achieved using PIN diode in GaAs technology. Stacking of transistor might increase the power handling capability which can be ensured after proper analysis. However, the power handling capability achieved in the designed SPDT switch is sufficient in many millimeter-wave applications.

2.7.6 Switching speed

Switching speed is the ability of switch to change it's state. More specifically, it is switching from off state to on sate or vice versa. Switching speed is especially crucial when the switch is used to change between transmit and receive modes of operation.

In case of deep saturation configuration, a considerable amount of minority carriers build up on the base node of the HBT because both of the junction is forward biased. The extra charge built on the base can slow down the transistor. Due to this reason, most of the RF circuits avoids deep saturation. For switches, when the transistor is turned off, the minority carrier must discharge before the device is totally turned off [23].

In the reverse saturated switch shown in figure 2.9, there is a quarter-wave transmission line at the base of transistor. There is a RF short circuiting capacitor at the other terminal of the quarter-wave transmission line. The quarter-wave bias line presents a large impedance at E band and low impedance at lower frequencies. The task of this quarter of line is to provide isolation from base to ground at the E band. So, the extra charge at the base node can easily flow to ground when the transistor is turned off. The charge flow is only limited by the current limiting resistance before the short circuiting capacitor. But the resistor does not cause severe problem as it has the small valued resistor of 30 Ω.

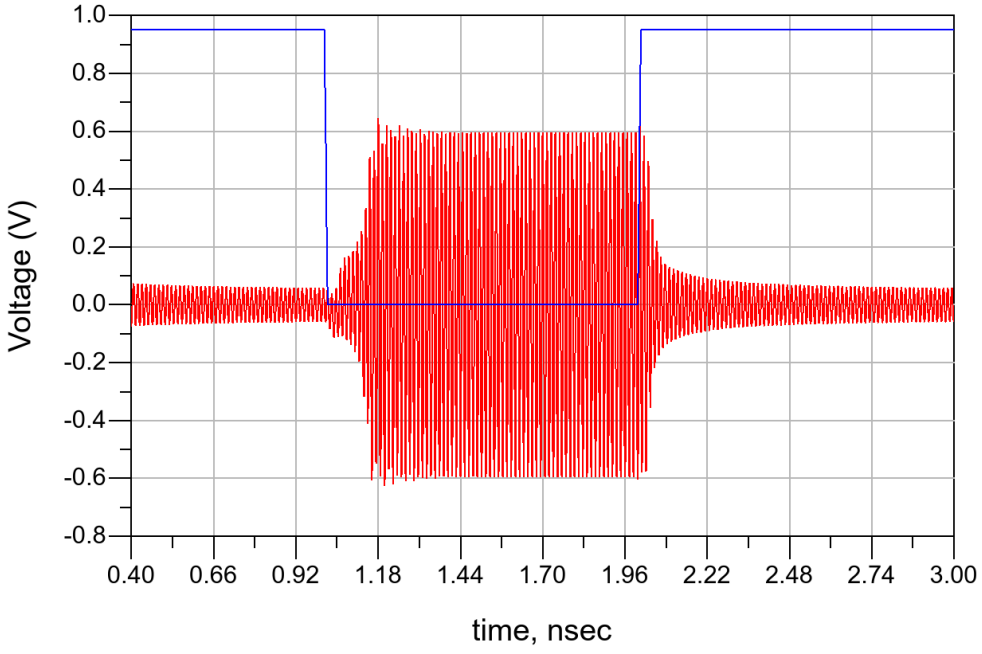


Figure 2.20: Transient response of reverse saturated shunt SPDT switch

Figure 2.20 shows the transient response of the reverse saturated SPDT switch. The switching time can be calculated from this figure. The turn on and turn off time

is 170 ps and 200 ps respectively. The result shows similar performance as in [29] where nFET was used and the switching time was 300 ps. So, it comparable to speed in CMOS technology. It is also quite similar to the performance with SiGe HBT in [25]. Therefore, deeply saturated switch with quarter-waave transmission line at the base can work properly from the switching speed point of view.

2.7.7 Evaluation

Table 1 compares the performance of the designed switches to other state-of-art millimeter-wave SPDT switches. A significantly low loss and high isolation has been achieved with both of the forward and reverse saturated quarter-wave shunt switches in this work. However, the switch with reverse saturated HBTs offers better insertion loss than the switch with forward saturated HBTs.

Table 1: Performance Comparison of Millimeter-Wave SPDT switches

Ref	Technology	Topology	Frequency Range(GHz)	Insertion Loss(dB)	Isolation (dB)	Return Loss(dB)	Pdc (mW)	P1dB (dBm)
This work	130nm SiGe HBT	$\lambda/4$ shunt rev. sat.	60-90	1-1.5	22.5-25	>10	7	18
This work	130nm SiGe HBT	$\lambda/4$ shunt for. sat.	60-90	1.6-2.3	22.5-25	>10	7	18
[21]	90nm SiGe HBT	$\lambda/4$ shunt rev. sat.	77-110	1.4-2.1	18-20	>10	8	19
[21]	90nm SiGe HBT	$\lambda/4$ shunt rev. sat.	82-110	2-2.8	18-20	>10	8	19
[22]	90nm SiGe HBT	$\lambda/4$ shunt rev. sat.	73-110	1.1-1.8	19-22	>10	5.9	17
[22]	90nm SiGe HBT	$\lambda/4$ shunt for. sat.	78-110	1.3-2.1	20-21	>10	5.9	17
[27]	90nm CMOS	traveling wave	50-94	3-3.5	27-35	>10	-	15
[28]	120nm BiCMOS	$\lambda/4$ shunt	85-105	2.3-3.5	20-21	>10	-	15
[29]	130nm SiGe PIN	Series shunt	50-78	2-2.7	28-35	>11	16.8	-
[24]	90nm SiGe PIN	$\lambda/4$ shunt	73-133	1.4-2	19-22	>10	-	24
[19]	GaAs PIN diode	Traveling wave	75-110	1.3-1.6	21-22	>10	-	-

The designed reverse saturated SPDT switch in this work shows better performance to those implemented in BiCMOS processes using SiGe HBTs. It also shows better performance than CMOS switches and competitive performance with those implemented in III-V technologies. However, the results presented in this work are pre-layout results. But still, the results are promising. Based on these results, quarter-wave shunt switch with reverse saturated HBTs may enable significant improvements to future silicon-based millimeter-wave systems.

The quarter-wave shunt switch with reverse saturated HBTs has been chosen for implementation due to it's better performance than forward saturated switch and the switch will be integrated to other circuits in the proposed transceiver system.

3 Millimeter-Wave Low Noise Amplifier Design

Low noise amplifiers (LNA) are critical building block in wireless receivers. Since LNA is the first block in the receiver path, the gain and noise figure from the LNA determines the noise figure of whole receiver . Therefore, low noise figure and high gain are critical requirements for the LNA design over the frequency band of interest. In this chapter, the given LNA specifications, some basic considerations related to design of millimeter-wave low noise amplifier such as stability, noise figure, gain and nonlinearity are discussed. A low noise amplifier for E-band is designed and post layout simulation results are shown.

3.1 LNA Specifications

Before starting the design of LNA, there were some requirements that are needed to be fulfilled by the targeted LNA. Table 2 shows the specifications of the target LNA. The gain should be as flat as possible within the specified bandwidth. Both noise figure and gain is defined for the center frequency of 75 GHz. The switch is connected to the input of LNA. The output of LNA is connected to the vector modulator. Therefore, LNA output should be matched to input of vector modulator.

Table 2: LNA specifications

Specification	Value	Unit
Gain	$\geqslant 25$	dB
Noise Figure	$\leqslant 6.5$	dB
Bandwidth	71-76	GHz
S11	$\leqslant -10$	dB
DC power	<35	mW

3.2 Noise Figure

Noise factor is the measure of degradation in signal-to-noise ratio between the input and output of the component and it is defined as

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{15}$$

where SNR_{in} and SNR_{out} represent the input and output signal-to-noise ratio respectively. Signal-to-noise ratio is the ratio of desired signal power to undesired noise power. Noise figure (NF) is the decible representation of noise factor and it is given by

$$NF = 10log(F) \tag{16}$$

3.2.1 Noise figure in cascaded system

In a typical microwave system, signal travels through several cascaded components and each of them degrades the signal-to-noise ratio to some extent. If the noise factor and gain of each stage is known, the total noise factor in the cascaded system can be found from the formula [33].

$$F_{cas} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{17}$$

Equation 17 shows that the total noise figure in the cascaded system is dominated by the characteristics of the first stage. For the best noise figure from the overall system, the first stage should provide low noise figure and sufficient gain performance. This is the motivation for a low noise amplifier at the first stage of the receiver chain. Efforts should be devoted to the design of the first stage since it is the most dominating in the chain.

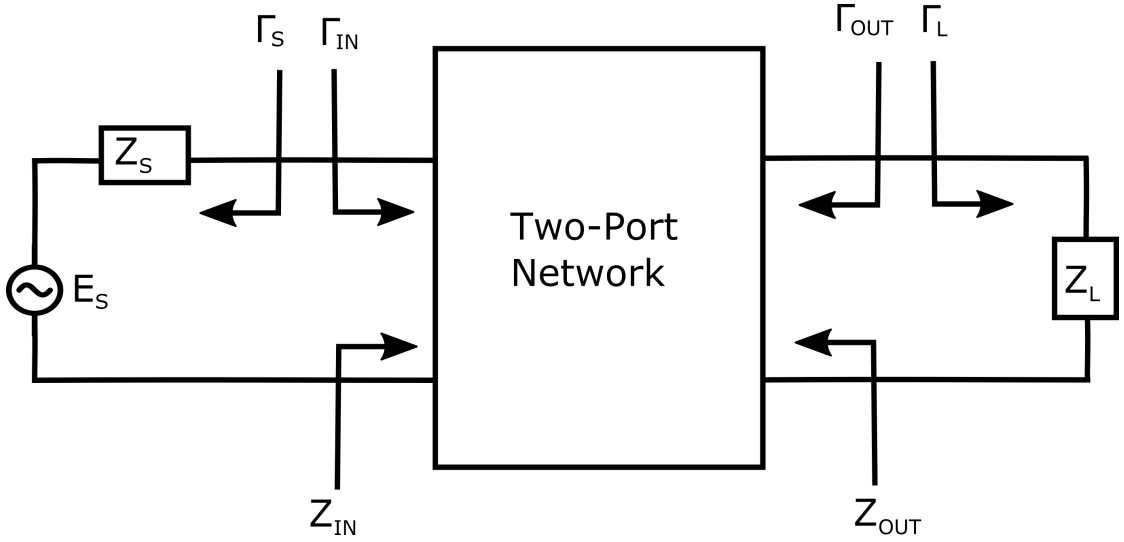


Figure 3.1: Important parameters used in stability analysis of two port network

3.3 Stability Analysis

Stability is the key consideration in amplifier design. Stability analysis is performed to determine whether the amplifier is stable at all the frequencies of interest. Figure 3.1 shows a general two port network. There is possibility of oscillation in this network if input or output port impedance has negative real part. This negative real part can cause the reflection coefficient to be larger than unity which can cause uncontrollable oscillation in this amplifier network. Stability of amplifier is dependent on the input and output matching networks. Two kinds of stability can be defined as follows

Unconditional stability: The network is unconditionally stable if magnitudes of both input and output reflection coefficients are less than one for all passive source

and load impedances that is $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$.
Conditional stability: The network is conditionally stable if magnitudes of both input and output reflection coefficients are less than one for certain range of passive source and load impedances. This is also called potentially stability.

3.3.1 Single stage stability

There is simple way to determine whether the amplifier is unconditionally stable or not. An amplifier is unconditionally stable if it satisfies the Rollet's stability conditions. This is called $K - \Delta$ test. These two conditions are defined as follows [33]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|} > 1 \tag{18}$$

and

$$\Delta = |S_{11}S_{22} - S_{21}S_{12}| < 1. \tag{19}$$

Not all CAD tools provide Δ as simulation parameter. In ADS keysight , another parameter called "StabMeas1" can be used which is defined as

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{20}$$

where B represents the StabMeas1. Therefore, in this case $K > 1$ and $B > 0$ are the corresponding conditions for unconditional stability. K and B are called stability factor and stability measure respectively. If he S-parameter does not satisfy these conditions, stability circles on Smith chart can be used to determine whether the amplifier is stable or not.

3.3.2 Multistage stability

The stability conditions defined above are applicable only for a single stage amplifier. Multistage amplifier can not be justified using these conditions. Because, in multistage amplifier the conditions $\Gamma_S < 1$ and $\Gamma_L < 1$ are no longer applicable. This is due to the fact that intermediate stages are terminated with active networks. So taking a multistage amplifier as single two port network and analyzing k-factor is not sufficient for overall stability [34].

There are some means to ensure that a multistage amplifier is stable. One approach in making the multistage amplifier stable is to design each stage for unconditionally stability. If all of the stages satisfy the k-factor conditions, then the amplifier is stable. However, this is a sufficient but not necessary condition. Because if an amplifier is designed in this way, it is very likely to provide a poor gain performance.

To overcome this problem a new stability test method is proposed in [35] which is based on Nyquist stability criterion. A potentially unstable device can be made unconditionally stable either by resistively loading the transistor or adding negative feedback. These techniques are very popular in broadband amplifier design. However,

these techniques are not recommended for narrowband amplifier design because of degradation of power gain, noise figure and so on [36].

There is always trade-off between gain and stability in potentially unstable devices. The higher the stability, the lower the attainable gain.

3.4 Constant-Gain Circle

Constant-gain circles are utilized on Smith chart to provide a graphical aid for designing an amplifier for a specified gain. In many cases, it is needed to match a transistor for specified gain which is less than the maximum obtainable gain. This kind of matching is done to widen bandwidth or to attain a specified gain. This can be done by designing input and output matching section to have less than maximum attainable gain. The design procedure is facilitated by plotting the gain circles on the Smith chart and placing the Γ_S or Γ_L along the circle of interest. The gain circles can be plotted using the equations provided in [33]. The center and radius for the input section gain circle is expressed by

$$C_S = \frac{g_S S_{11}^*}{1-(1-g_S)|S_{11}|^2} \tag{21}$$

$$R_S = \frac{\sqrt{1-g_S}(1-|S_{11}|^2)}{1-(1-g_S)|S_{11}|^2} \tag{22}$$

and the center and radius for the output section gain circle is expressed by

$$C_L = \frac{g_L S_{22}^*}{1-(1-g_L)|S_{22}|^2} \tag{23}$$

$$R_L = \frac{\sqrt{1-g_L}(1-|S_{22}|^2)}{1-(1-g_L)|S_{22}|^2} \tag{24}$$

where g_s and g_L represents the normalized gain factors given by

$$g_S = \frac{G_S}{G_{Smax}} = \frac{(1-|\Gamma_S|^2)(1-|S_{11}|^2)}{|1-S_{11}\Gamma_S|^2} \tag{25}$$

$$g_L = \frac{G_L}{G_{Lmax}} = \frac{(1-|\Gamma_L|^2)(1-|S_{11}|^2)}{|1-S_{11}\Gamma_L|^2}. \tag{26}$$

These equations are valid for the unilateral device where $|S_{12}| = 0$. In reality, small amount of error can appear due to this approximation.

Figure 3.2 shows the gain circles plotted on Smith chart. If Γ_S is placed along any of the circles, that specified amount gain can be achieved whereas placing Γ_S inside any circle produce more gain than that specified circle. For example, if a Γ_S is placed along the circle that has gain of 5 dB, the circuit will have maximum attainable gain gain of 5 dB. The circle closer to the center has higher gain.

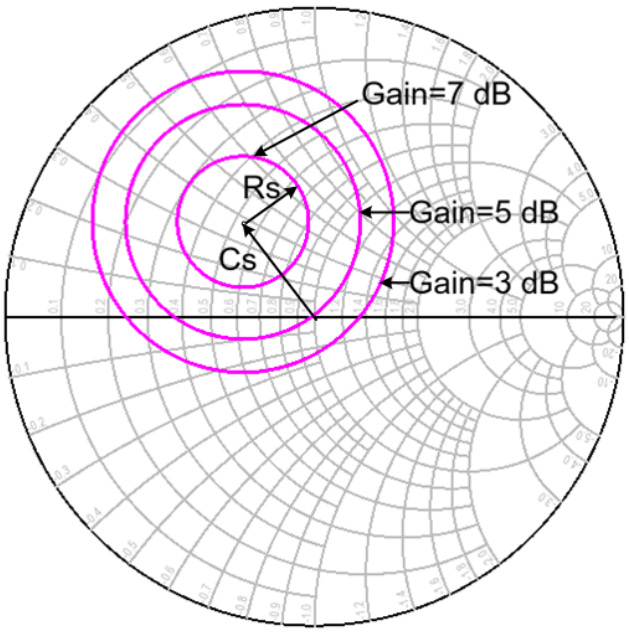


Figure 3.2: Constant-gain circle on the Smith chart

3.5 Constant-Noise Circle

Noise figure plays an important role in microwave circuits. Low noise figure and high gain are always desired characteristics of a microwave circuit, specially in low noise amplifier. But it is not possible to attain both the minimum noise figure and the maximum gain simultaneously. There is always a trade-off between gain and noise figure. Constant noise circles and gain circles are used to select the suitable trade-off between gain and noise figure.

As shown in reference [33], the noise figure of two port network can be written as

$$F = F_{min} + \frac{R_N |Y_s - Y_{opt}|^2}{G_s} \tag{27}$$

where Y_s is the source admittance presented to transistor, Y_{opt} is the optimum source admittance that results in minimum noise figure, F_{min} is the minimum noise figure of transistor attained when $Y_s = Y_{opt}$, R_N is the equivalent noise resistance of transistor and G_s is the real part of source admittance.

From the above equation, it is clear that the minimum noise figure of a single transistor will be attained if the source admittance is equal to the optimum admittance of the transistor. Y_s and Y_{opt} can be expressed in terms of reflection coefficient as follows

$$Y_s = \frac{1 - \Gamma_s}{Z_o(1 + \Gamma_s)} \tag{28}$$

$$Y_{opt} = \frac{1 - \Gamma_{opt}}{Z_o(1 + \Gamma_{opt})} \tag{29}$$

According to reference [33], the center and radii of constant noise circles can be derived as follows

$$C_F = \frac{\Gamma_{opt}}{N+1} \tag{30}$$

$$R_F = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1} \tag{31}$$

where the noise figure parameter N is defined as

$$N = \frac{|\Gamma_s - \Gamma_{opt}|^2}{1-|\Gamma_s|^2}. \tag{32}$$

Figure 3.3 shows the constant-noise circles on the Smith chart. To design for a specific noise level one would then place Γ_S along the noise circle of interest.

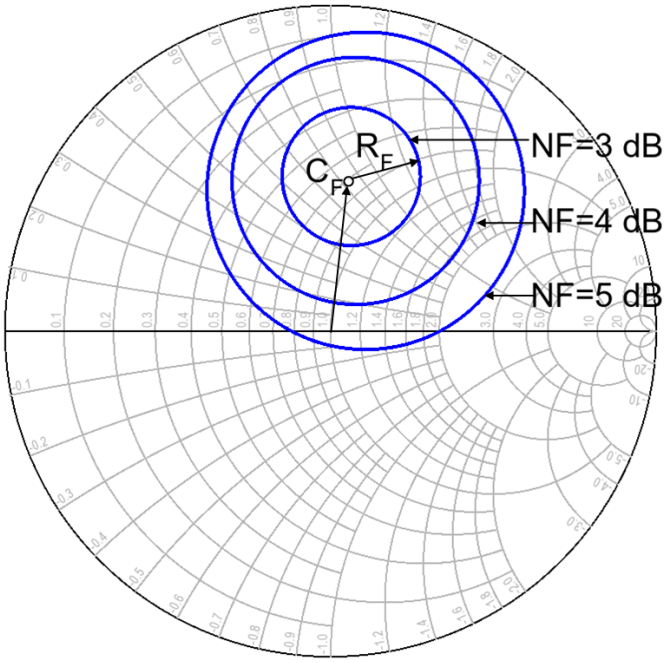


Figure 3.3: Constant-noise circle on the Smith chart

Figure 3.4 shows the noise circles and gain circles plotted on the same Smith chart. Now, from this chart, gain and noise trade-off can be selected easily. To obtain a noise figure of 3 dB and gain of 5 dB one can place the Γ_S inside the shaded region. One can go towards the center of gain circles to attain more gain while attaining higher noise figure.

3.6 Non-linearity

Non-linearity is one of the important properties of practical amplifiers. Even though a transistor can be considered fairly linear for small signal, it will exhibit nonlinear behaviour at large input signal levels.

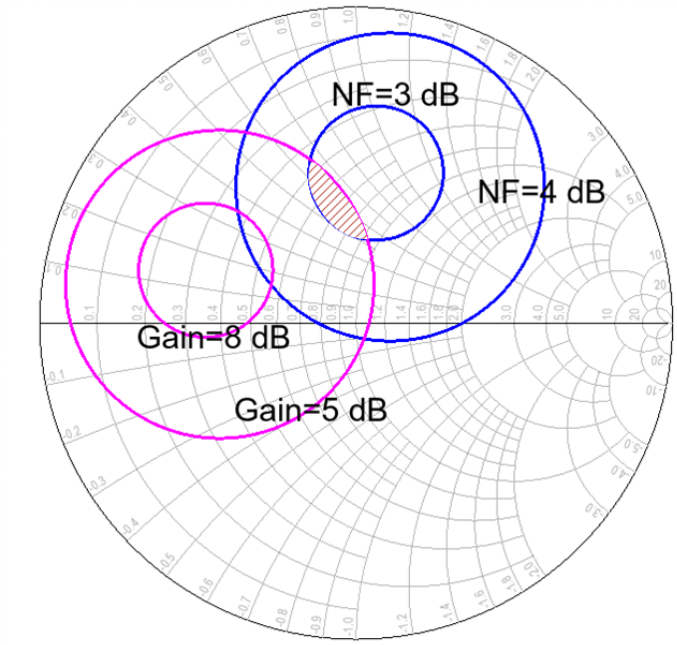


Figure 3.4: Noise circles and gain circles plotted on the Smith chart

In general the output response of a nonlinear device or circuit can be modeled as Taylor series in terms of the input voltage as

$$V_0 = a_0 + a_1 V_i + a_2 V_i^2 + a_3 V_i^3 + ... \tag{33}$$

Practical devices will have series expansion with several nonlinear terms which results in nonlinear characteristics from the devices.

3.6.1 Gain compression

In most amplifiers a_3 in Equation 33 is negative. So the output will be reduced at large signal levels which causes drop in the amplifier gain. This phenomenon is called gain compression. The 1-dB compression point is defined as the power level when output power has decreased by 1 dB compared to the ideal linear characteristics. This power level is generally denoted by P_{1dB}. This power level can be denoted either in terms of input power (IP_{1dB}) or output power (OP_{1dB}). Generally, gain compression is the result of saturation of transistors or active devices. Figure 3.5 shows the typical amplifier response and 1-dB gain compression point.

3.6.2 Third-order intercept point

The third-order intercept point is the hypothetical point where the third order output power and linear output power would be equal. This never happens in reality but still it is a good measure of linearity. This point is denoted as $IP3$. Third-order intercept point can be denoted as input power level ($IIP3$) or output power level ($OIP3$). Figure 3.5 shows the definition of IP3.

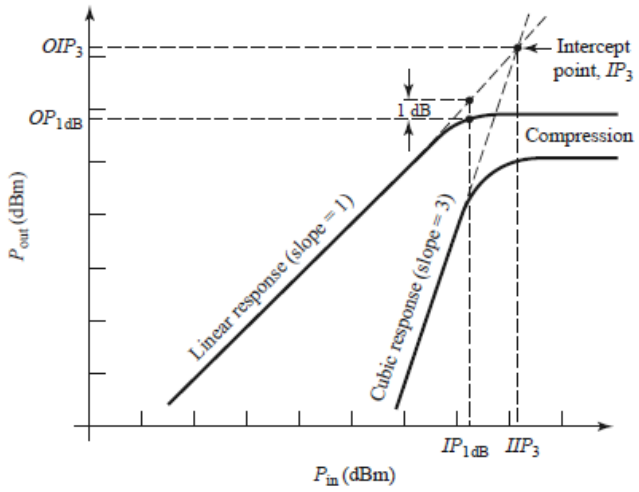


Figure 3.5: Definition of 1dB compression point and third order intercept point [23]

3.6.3 IP3 in cascaded System

Usually, a single stage amplifier can not provide sufficient gain. To achieve required gain, several stages need to be cascaded. The total $IIP3$ of a cascaded system can be expressed as follows

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} \tag{34}$$

where $IIP3_i$ and G_i are the input-referred $IP3$ and the power gains, respectively, of each individual stage of the amplifier [37]. It is clear from this equation that linearity of later stages will dominate the overall linearity of the system. Therefore, the linearity of the output stage should be maximized in order to maximize the linearity of the overall cascaded system.

3.7 Emitter Degeneration

An additional inductor L_E can be inserted at emitter as shown in Figure 3.6(a). Figure 5.6(b) shows the small signal model of a transistor with a degeneration inductor L_E. This degeneration inductor is mainly used in low noise amplifier to achieve simultaneous gain and noise matching. Degeneration improves the gain and noise matching simultaneously by bringing the gain circles and noise circles closer.

Even though the transistor is fairly linear for small input signals, the current gain, β, of the bipolar transistor will vary as the collector current varies. This will in turn change the gain of the amplifier and cause a non-linear response. This emitter degeneration inductor L_E makes the amplifier gain less dependent on the value of β and thus makes the transistor linear for a larger range of input voltages. The cost of this improvement in linearity is loss of gain [38].

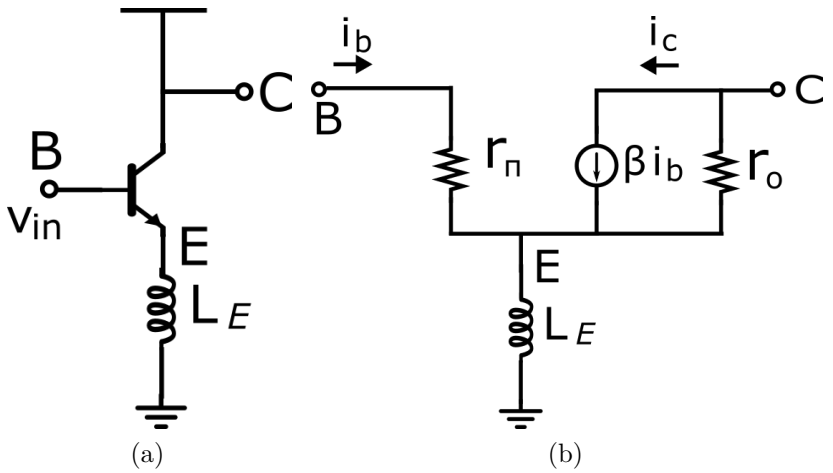


Figure 3.6: (a) Common-emitter amplifier with degeneration inductor. (b) small signal model with degeneration inductor

In addition, the degeneration introduces negative feedback in the transistor, thus improving the stability of the transistor, which is the another reason of using degeneration inductor at the emitter [38]. An unconditional stability can be achieved by sufficient emitter degeneration.

Furthermore, input impedance of transistor can be modified by this inductor. Another advantage of emitter degeneration is that the circuit becomes less sensitive to temperature and process variations [38].

3.8 Transmission Lines

There are several advantages of using transmission line in matching networks in MMIC design. Reactance of transmission line is more predictable and less affected by surroundings than the lumped spiral inductor. Another important characteristic of transmission line is scalability. If a transmission line is modeled carefully, different lengths of transmission line can be used without modeling for each length. On the other-hand, lumped element needs to be modeled individually for each size which is very time consuming. Transmission line can be designed to obtain specific value of characteristic impedance to improve the performance. Equivalent circuit model for an incremental length of transmission line is shown in figure 3.7 where R is the series resistance per unit length, L is the series inductance per unit length, G is the shunt conductance per unit length, C is the shunt capacitance per unit length and Δz is the incremental length. Inductive quality factor (Q_L) and capacitive quality factor (Q_C) are two figure of merits of transmission lines and they determine the performance of a transmission line. Q_L and Q_C can be defined in terms of model parameters as follows

$$Q_L = \frac{\omega L}{R} \tag{35}$$

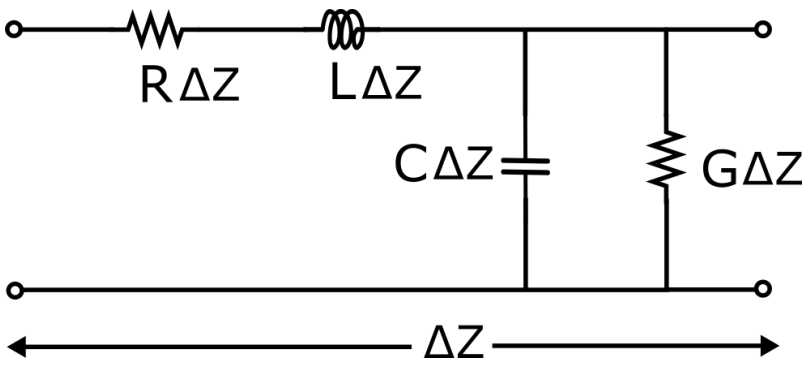


Figure 3.7: Equivalent circuit model for an incremental length of transmission line

$$Q_C = \frac{\omega C}{G} \tag{36}$$

where ω is the frequency in radian. As it is stated in [39] that the Q_L is more important than the Q_C when transmission lines are used to match the intrinsic capacitance of the transistor. Some widely used transmission line types will be discussed in the subsequent section briefly.

3.8.1 Coplanar waveguide

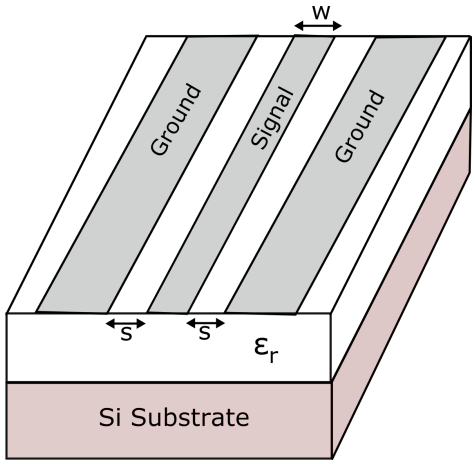


Figure 3.8: Coplanar waveguide structure

Figure 3.8 shows the general coplanar waveguide in silicon technology. The width of signal line is w and spacing between the signal line and ground line is s. To realize different characteristic impedances for the coplanar waveguide, the parameters w and s can be adjusted. A wider center conductor leads to a lower conductor losses. Q_L is dependent on the spacing s between signal and ground. As a result, the spacing s can be changed to obtain a higher inductive quality factor Q_L which is very useful characteristic of coplanar waveguide. However, as the distance between the signal and ground lines increases, substantial loss arises due to low resistivity silicon substrate and G becomes higher.

3.8.2 Microstrip line

Figure 3.9 shows the general microstrip line in silicon technology. Microstrip line is realized by using top metal layer as conducting strip and lower metal layer as ground plane. The width of signal line is w and distance between the conducting strip and the ground plane is h.

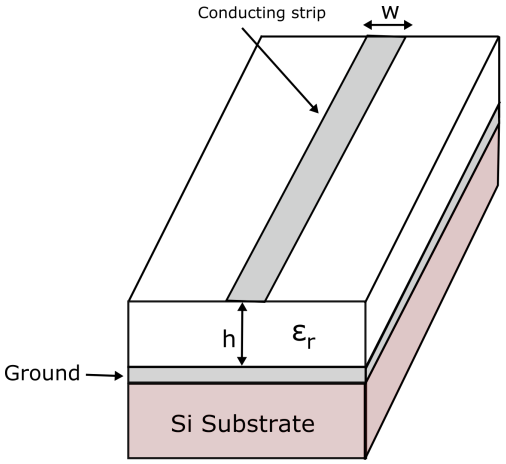


Figure 3.9: Microstrip transmission line structure

Microstrip line offers mainly two advantages. First, this structure decreases the effect of the lossy silicon substrate. Second, modeling of microstrip line is easier and more reliable than the coplanar waveguide. However, for microstrip lines it is not possible to increase L arbitrarily by increasing the distance between the signal line and the ground plane, because the distance between the topmost and the bottommost metal layers is fixed for a certain technology. In addition, using bottom metal layers as the ground plane causes high conductive losses due to the fact that bottom metal layers are thinner.

3.8.3 Slow-wave coplanar waveguide

Both microstrip line and coplanar waveguide have respective advantages and disadvantages. In the conventional coplanar waveguide, the electromagnetic field penetrates into the silicon substrate which causes significant substrate loss. On the other-hand, microstrip line provides immunity against lossy silicon substrate as there is a ground plane beneath the conducting layer. Increasing Q_L in microstrip is not as easy as in coplanar waveguide. To utilize the advantages of both the coplanar and microstrip lines, a new structure can be formed as shown in Figure 3.10.

This is a coplanar structure with a metal shield implemented at the lower metal layers. Resulting structure is called as slow-wave co-planar waveguide (S-CPW). Metal shield prevents electromagnetic fields from penetrating into the lossy substrate [40], [41]. Inductive quality factor remain same as in the regular coplanar waveguide and the capacitive quality factor increases as the substrate is shielded now. In

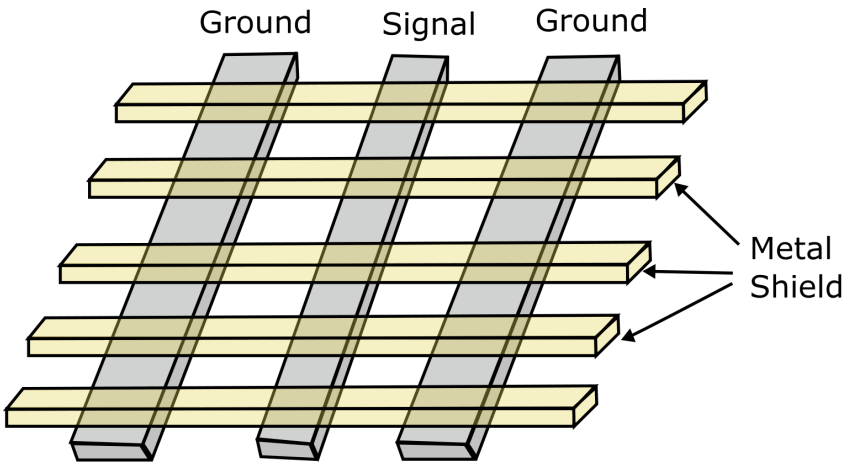


Figure 3.10: Slow-wave co-planar wave guide structure

addition, S-CPW structure presents slow-wave effect, and therefore the effective dielectric constant is increased and the wavelength of the propagating signal is decreased. Therefore, it is possible to use shorter line for matching and save silicon area. However, modeling of S-CPW is more complex than microstrip line.

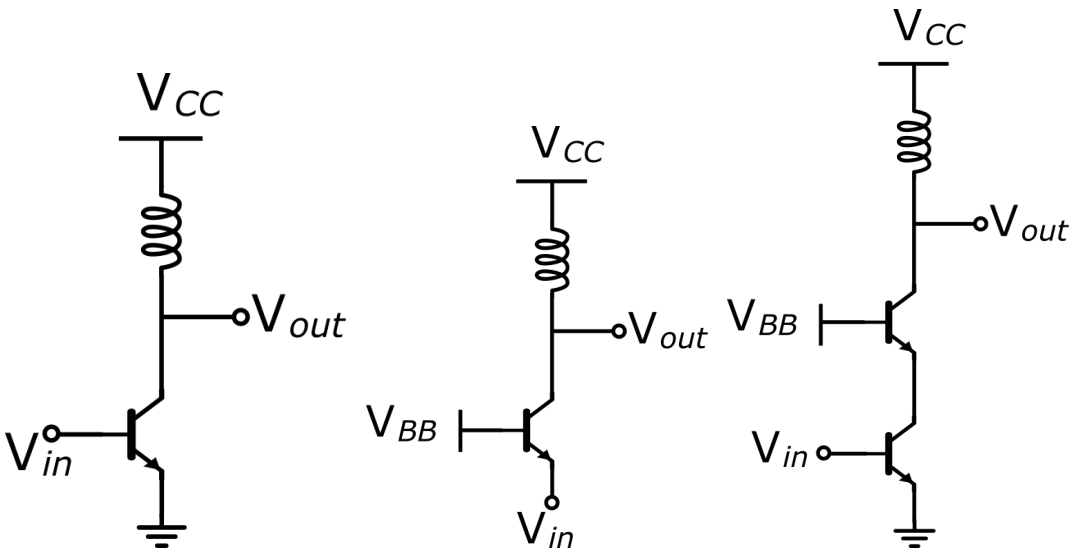
3.9 Amplifier Topology

Choosing an appropriate topology plays an important role in LNA design. There are three commonly used topologies for LNA design. They are the common-emitter (CE), common-base (CB) and cascode topology shown in Figure 3.11. A comparison of some of the most important parameters of these topologies are shown in Table 3 [42].

Table 3: Comparison of commonly used LNA topologies

Parameter	Common-emitter	Common-base	Cascode
Gain	Moderate	Lowest	Highest
Noise Figure	Lowest	Rise rapidly with Frequency	Slightly higher than CE
Linearity	Moderate	High	Potentially Highest
f_{3dB}	Low	Fairly High	High
Reverse Isolation	Low	High	High
Stability	Requires compensation	Higher	Higher

The cascode topology offers the highest gain with higher stability. In addition, it is nearly unilateral so that it gives a good reverse isolation, and therefore matching becomes simpler [43]. However, the cascode amplifier adds complexity in circuits as it needs higher supply voltage. In addition, there is a large parasitic capacitance (C_p) on the shared junction between two transistors as shown in Figure 3.12(a). At high



(a) Common-emitter (b) Common-base (c) Cascode

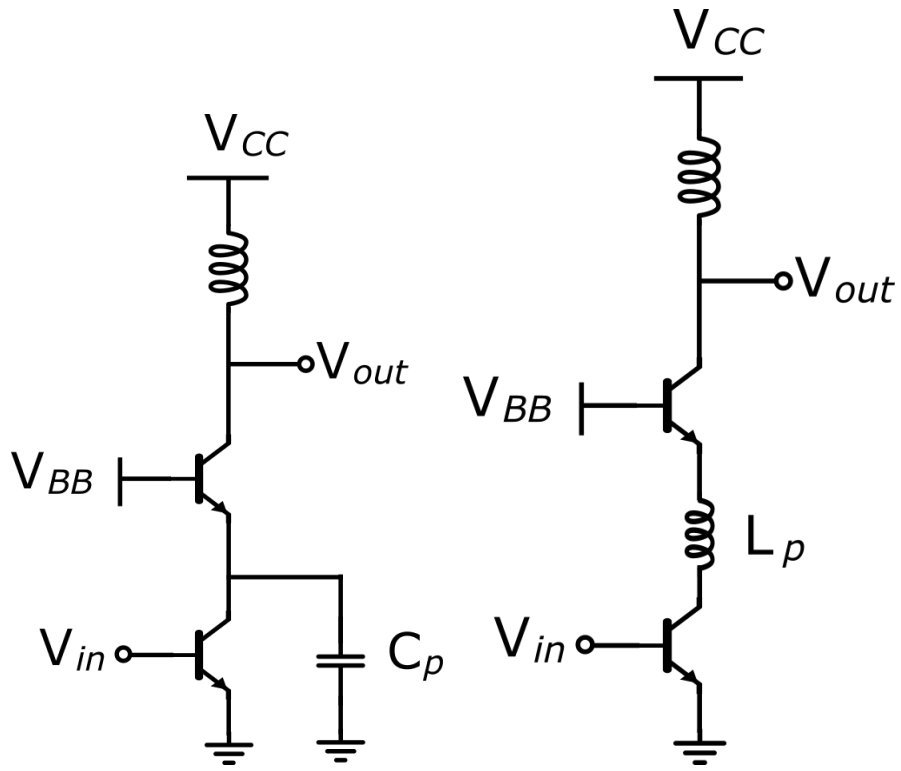
Figure 3.11: Commonly used LNA topologies

frequencies, this capacitance shows a low impedance and reduce the gain of amplifier. This capacitance can be resonated out by placing a series inductor between the transistor as shown in Figure 3.12(b) and therefore making the modeling of cascode stage difficult.

The common-emitter stage has the lowest noise of all three topologies and moderate gain and linearity. The common-base stage provides high linearity and reverse isolation. The common-base configuration offers easy matching as the input impedance of the transistor in simply $\approx \frac{1}{g_m}$. However, a high noise figure and low gain make it less suitable for LNA design.

3.10 Selecting Topology

Most important characteristics of commonly used LNA topologies are shown in Table 3. As significantly high gain is required, it is necessary to cascade several stages. Different topologies provide different advantages. So it is beneficial to combine different amplifier topologies to get corresponding advantages. The common-emitter amplifier has been used at the first stage as it provides low noise figure. A cascode amplifier offers high gain and higher noise figure than common emitter topology. Cascode configuration has been used at the second stage due to two important facts. Firstly, it has high gain and secondly the noise figure in the second stage is not that critical if the first stage has sufficient gain. As the LNA needs to drive the differential vector modultor, a differential cascode stage has been used to provide differential signal.



(a) cascode with parasitic capacitance (b) inductor in shared junction

Figure 3.12: Parasitic capacitance in cascode stage

3.11 Choosing the Bias Point

As discussed in section 3.2.1 noise from the subsequent stages are suppressed by the relative gain of the first stage. This requires that the gain of the first stage is significantly high. The noise figure of the first stage is dominating. Gain and noise figure heavily depends on the biasing of transistors. Therefore, by careful selection of the bias points of the transistors, it is possible to obtain better gain and noise figure at mm-wave frequencies.

A lower noise figure can be obtained at lower bias point but the obtainable gain is also lower. As the bias voltage goes higher, the obtainable gain and noise figure increase rapidly. Therefore, a lower bias voltage was selected for the common-emitter stage to keep the noise figure low and a comparatively higher bias voltage was chosen for the cascode stage to achieve higher gain.

3.12 Matching Network Design

The impedance matching network needs to be designed after careful selection of LNA topology and biasing voltage. Impedance matching plays a great role in most of the circuit design. Matching network is designed either to achieve the maximum power transferred from source to load or to achieve desired noise figure from the circuit.

The first one is called power matching and the later one is called noise matching. In the design of low noise amplifier both of matching are critically important. Noise matching is done in order to achieve lower noise figure from the circuit and power matching is done to provide sufficient signal gain. It requires very careful design consideration to obtain the desired amount of gain and noise figure. This section deals with different matching principles used in the design of targeted low noise amplifier.

3.12.1 Input matching principle

Input matching requires careful attention in LNA design. This section describes input matching principle of a low noise amplifier. An effective way of designing the matching network is using the available gain, noise and source stability circles of the input transistor drawn on a Smith chart. Figure 3.16 shows the elements of input matching network of first stage LNA. The noise circles, gain circles, stability circle and the the corresponding points after each element on the Smith chart are shown in Figure 3.17.

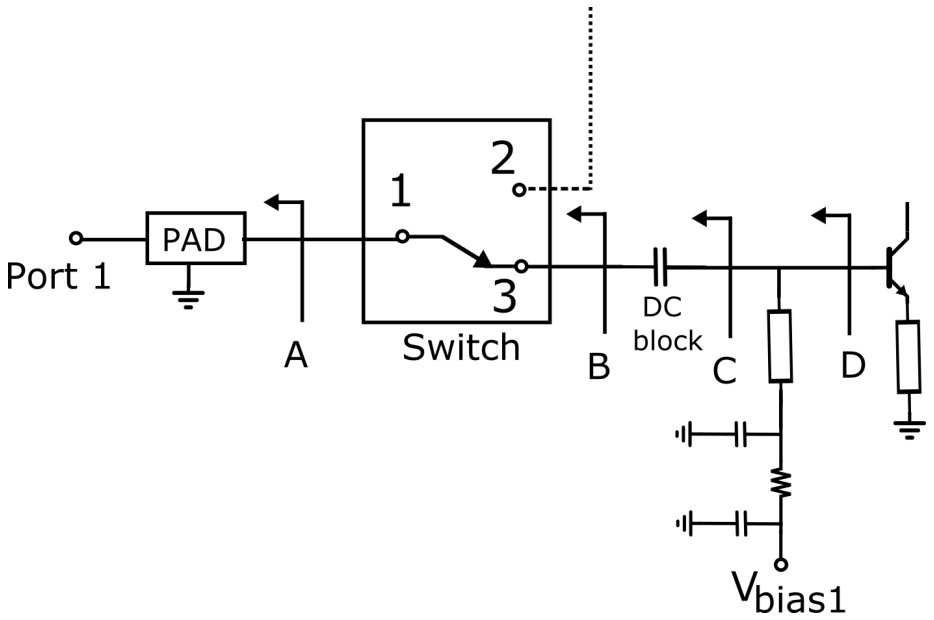


Figure 3.13: Input matching network of the low noise amplifier

The RF pad has been considered as the first element in the input matching network and the corresponding point on the Smith chart is A. As there is a SPDT switch before LNA, the switch is consider as the input matching element for the LNA. This switch is considered as a single pole single through(SPST) switch because the other arm of the switch is in off-state. This switch moves the impedance from A to B on the Smith chart. The next element is DC block capacitor that blocks the DC from the supply towards the Port1. Ideally, it is short for desired mm-wave frequencies. However, in this design DC block capacitor was used also as matching element. It

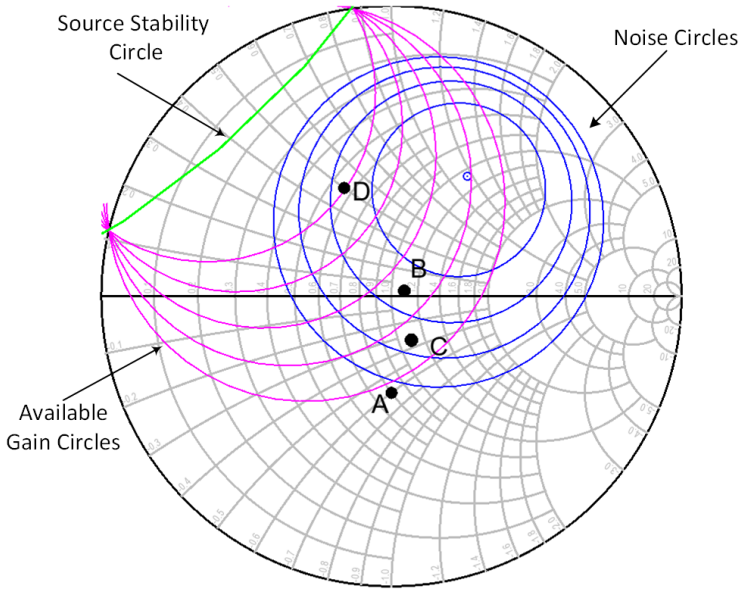


Figure 3.14: Input matching principle of a low noise amplifier using noise, gain and stability circles the Smith chart

moves the impedance point from B to C on the Smith chart. Biasing network is placed at the last position and it is used to reach the final point of input matching. It corresponds to the point D on the Smith chart. To attain higher gain impedance was moved from point C to point D. At this point desired noise and gain matching is achieved. For better noise figure one can move towards the center of the noise circle. Therefore, using noise, gain and stability circles one can choose the desired noise and gain from the Smith chart. Emitter degeneration is used to achieve simultaneous gain and noise match. The emitter degeneration is realized by a microstrip-transmission line. The degeneration inductor brings the gain circles and noise circles closer.

3.12.2 Interstage matching using transformer balun

Interstage matching was designed so that the output of first stage matches to the differential input of the second stage. The interstage matching network is shown in Figure 3.18. The output from the first stage is single ended and the differential cascode stage requires balanced signal at input.

Conversion of a single ended signal to a differential signal is done by the transformer balun. In addition to the single ended to differential conversion, the transformer serves some other important purposes. The transformer is used as an impedance matching element. The transformer provides bias points through the center-tapped primary and secondary windings [44]-[45]. In this design, bias voltage, V_{bias2} to the second stage is provided through the balun transformer. The primary and secondary of the transformer were realized by top two metal layers as shown in Figure 3.19. If the center point of both the primary and secondary are used to bias, the DC block capacitor can me eliminated. In addition to the transformer, DC block capacitor,

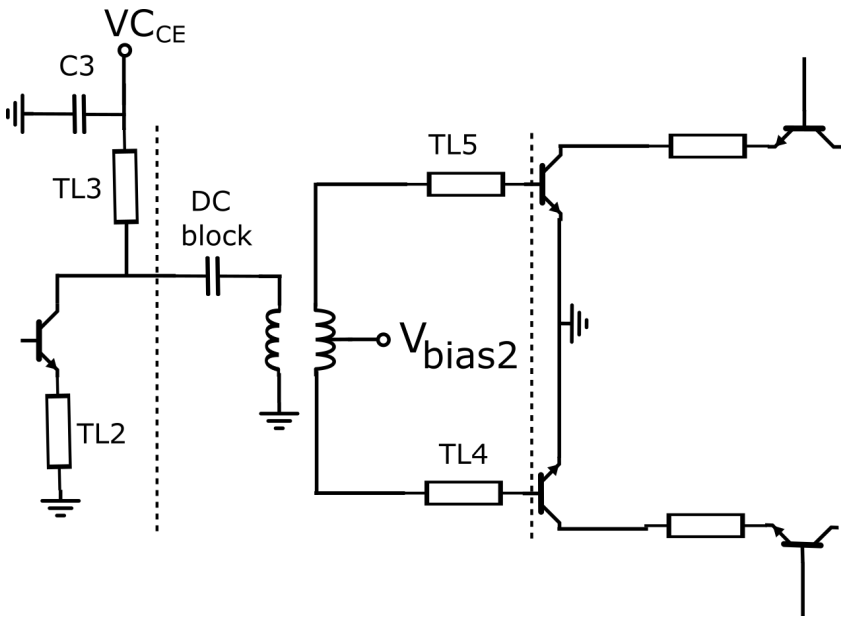


Figure 3.15: Interstage matching network

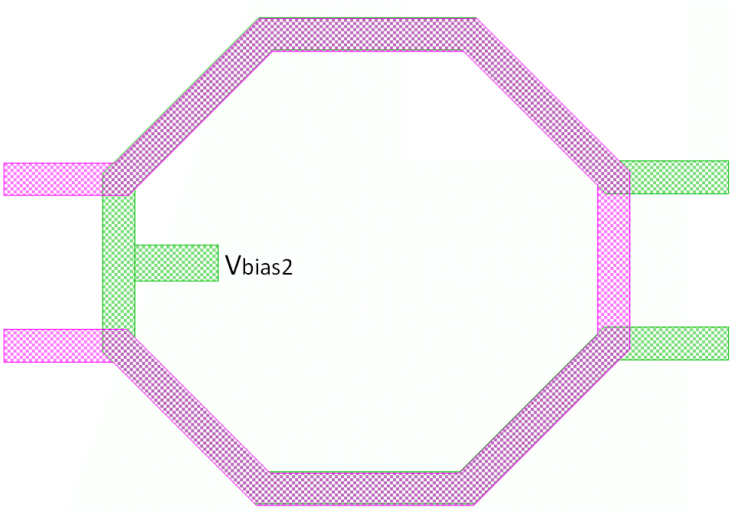


Figure 3.16: Realization of transformer balun by topmost two metal layers

TL4 and TL5 are used as the matching element. An RF choke was realized by a quarter-wave transmission line TL3 together with a short circuiting capacitor C3.

The most important parameter for output stage is the gain. Noise of the output stage is not of critical importance. However, the first stage can not totally suppress the noise contribution from the second stage and therefore, the noise also has been taken into account. To obtain a significantly high gain, a higher bias voltage of 880 mV has been chosen.

3.12.3 Output matching

The output of second stage of LNA is connected to a differential vector modulator. As the vector modulator is differential, no transformer balun was used. Figure 3.20 shows the output matching network of the LNA. Here, TL10 and TL11 are used for the DC supply as well as impedance matching.

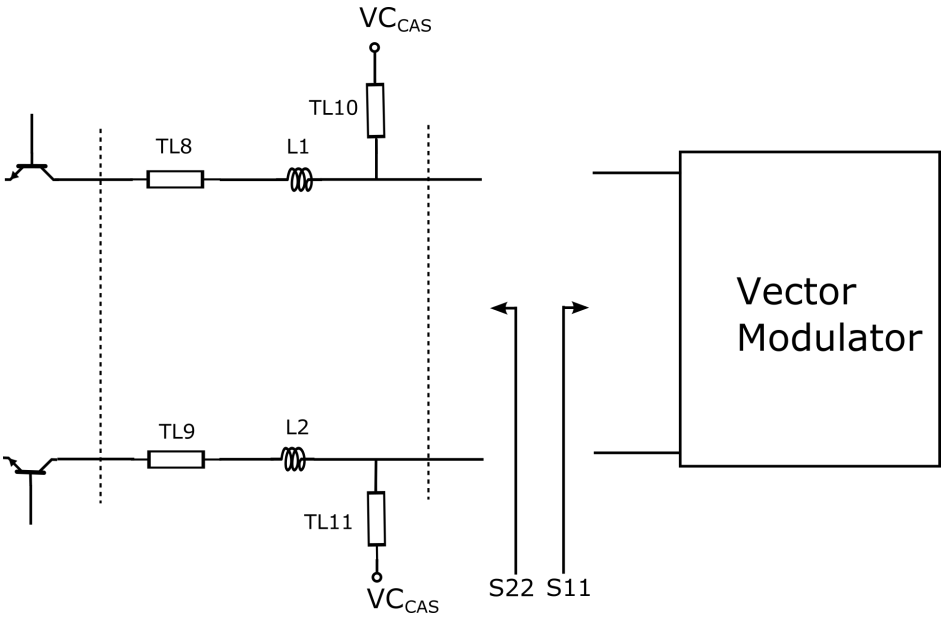


Figure 3.17: Matching network between LNA and vector modulator

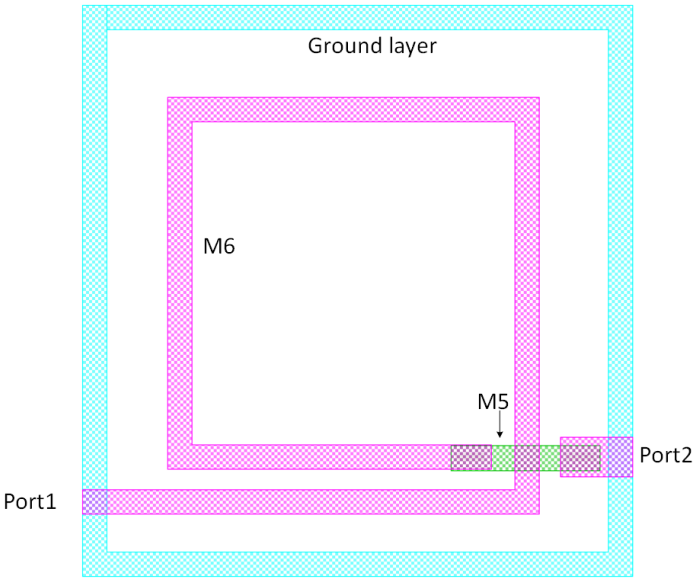


Figure 3.18: Matching network between LNA and vector modulator

Although a transmission line and a series inductor moves same way on the Smith

chart, a small length of transmission line (TL8, TL9) was used to facilitate the layout design. Only transmission line could be used instead of inductor but it would take larger area. A one turn inductor has been used and ADS Momentum was used to perform the electromagnetic simulation. The topmost metal, M6 has been used to design the inductor. An underpass with the fifth metal layer (M5) was used to connect the M6 to the port2. These two metal layers are directly on top of one another, so making the under-pass narrower would potentially reduce the parasitic capacitance. However, this effect was small as the underpass is very small. The ground layer was used to increase the simulation accuracy by providing a well defined return current path. The layout view of the inductor is shown in Figure 3.21.

3.13 Bias Circuit Design

The biasing was implemented by a current mirror as shown in Figure 3.22. The biasing circuit provides stable bias for the amplifier. The reference current, I_{REF} is set by the resistor R_1. The current I_{OUT} controlled by the reference current I_{REF}. As the emitter area of Q2 is A times the area of the Q_1, the current through the Q_2 is A times the current in the Q_1. The purpose of the resistors at the base of transistors is to provide high impedance path for RF signal. It also makes the circuit more stable against the temperature and process variation. The value of resistance at the base of transistor Q_1 is A times the resistance at the base of Q_2. The area of the RF transistor Q_2 was selected to be twice the area of the DC transistor Q_1. A resistance value of 20Ω was set for R_2. So the value of R_1 became 40 Ω.

$$R_1 = R_2 * A \tag{37}$$

$$R_1 = 20 * 2 \tag{38}$$

3.14 Post Layout Simulation Results

Post layout simulation results are shown and analyzed here to evaluate the performance of the designed low noise amplifier for E-band. Figure 3.23 shows the simulated s-parameters of LNA from 60 to 100 GHz. The LNA shows a peak gain of 26 dB at 75 GHz and a 3 dB bandwidth of 12 GHz from 68.7 GHz to 82.7 GHz. The result is in line with the desired requirements. The input return loss is greater than 15 dB at 75 GHz. The LNA shows reverse isolation (S_{12}) better than 54 dB for the whole E-band frequency range(not shown).

The noise figure is another important parameter to characterize a low noise amplifier. Figure 3.24 shows the simulated noise figure of the amplifier. The result shows 6.4 dB noise figure at 75 GHz and less than 7 dB from 67 GHz to 86 GHz and it is almost flat in this frequency range.

The simulated stability factor (K) and stability measure (B) are shown in Figure 3.25. The stability factor and stability measure are greater than one and zero respectively

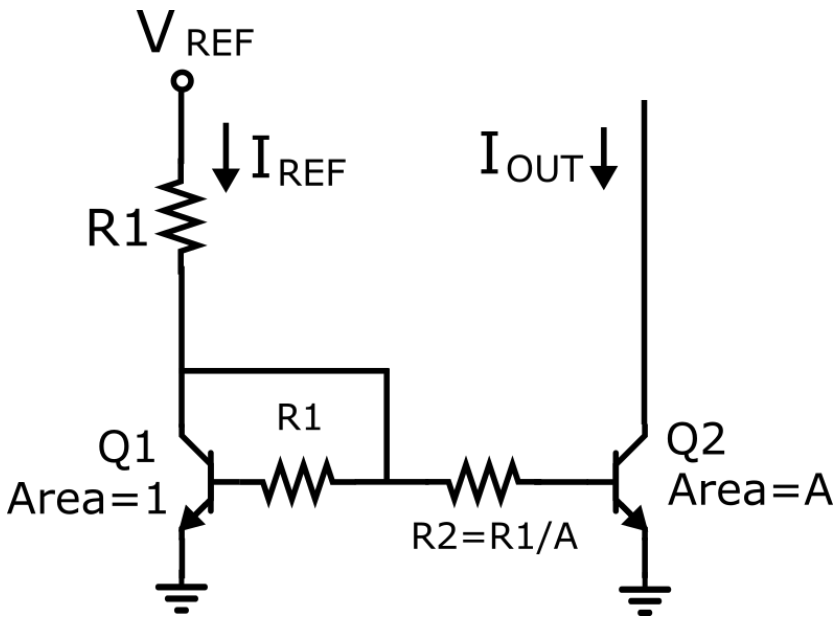


Figure 3.19: Current mirror for stable bias to amplifier

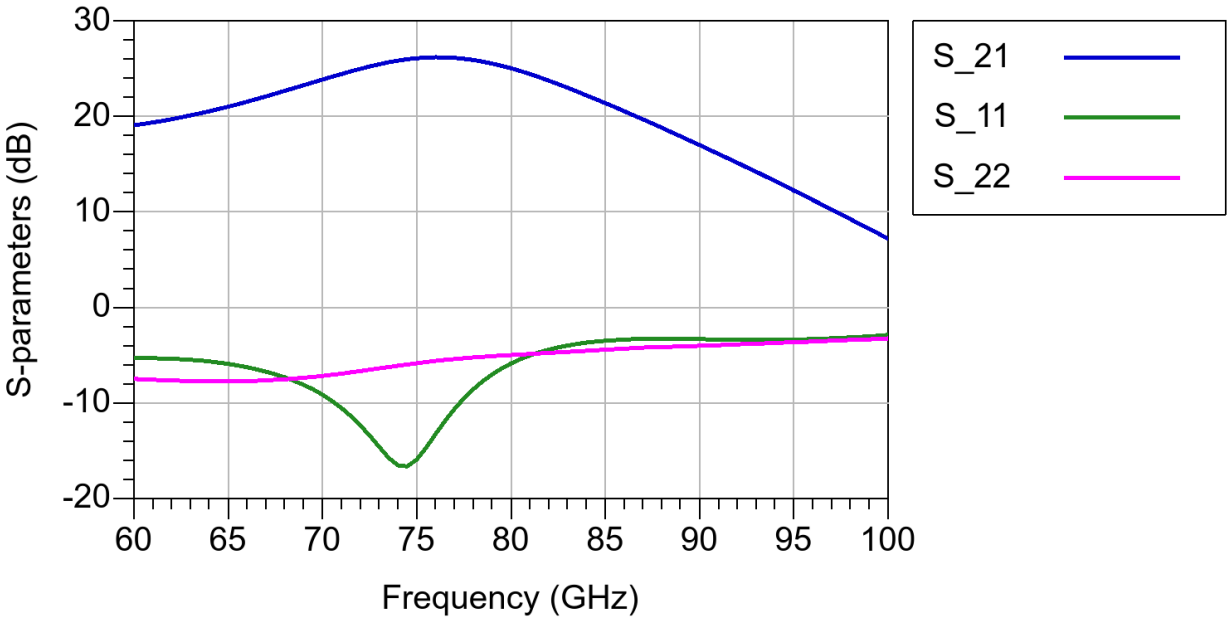


Figure 3.20: Simulated s-parameters of the E-band LNA

that are the necessary conditions for unconditional stability. Figure 3.26 also shows the source and load stability circles of the amplifier and all the circles are outside the unit circle ($\Gamma = 1$) which represents the unconditional stability of the amplifier. As each stage was designed with unconditional stability, there is no instability in the interstage node of the amplifier.

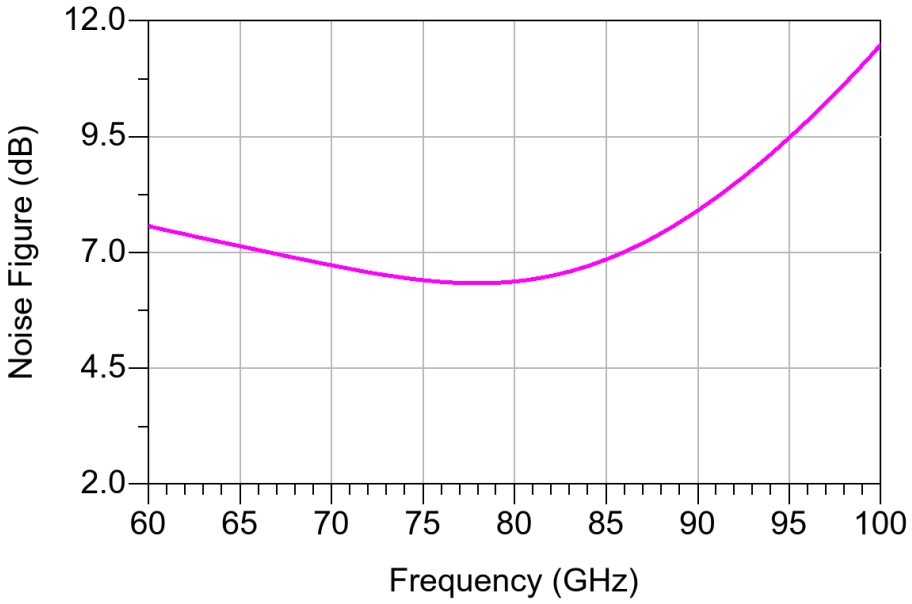


Figure 3.21: Simulated noise figure of the E-band LNA

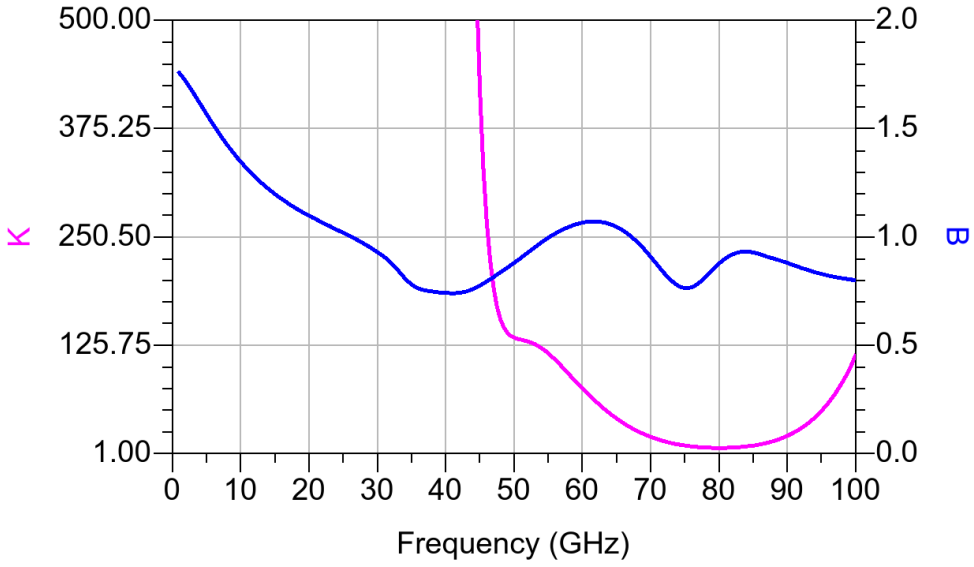
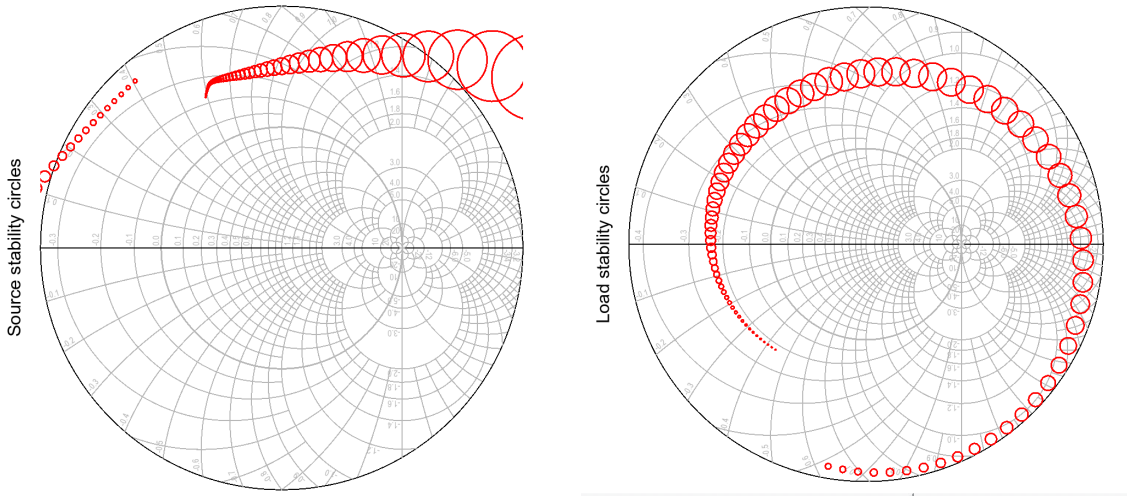


Figure 3.22: Simulated stability factor and stability measure of the E-band LNA

The simulated output 1 dB compression point is shown in Figure 3.27. The amplifier achieved a value of 5.5 dBm for output 1 dB compression point at 75 GHz. The low noise amplifier consumes 33.5 mW of DC power. More specifically, the common-emitter first stage consumes 4.3 mW and the cascode second stage consumes 29.2 mW including all the current mirrors.



(a) (b)

Figure 3.23: Simulated source stability circles [a] and load stability circles [b]

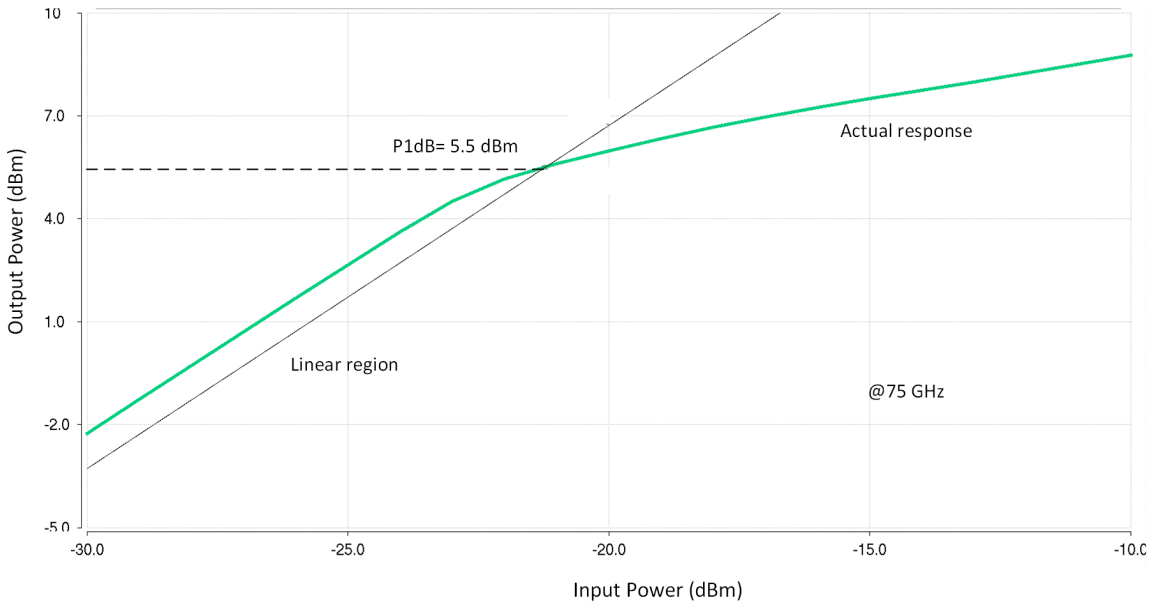


Figure 3.24: Simulated 1 dB compression point of the E-band LNA

3.15 Performance Comparison of the Designed E-Band LNA

Table 4 compares the simulated performance of the designed E-band LNA to other published state-of-art E-band LNAs. As can be seen, the 2-stage amplifier with common-emitter first stage and cascode second stage amplifier designed in this work achieves a significantly high gain and a reasonable noise figure. The DC power consumption in the designed LNA is considerably low compared to most of the other works. The designed LNA achieves the highest output 1 dB compression point (OCP_{1dB}) among all the other published works.

Table 4: Performance Comparison of the E-Band LNA

Ref	Technology	Topology	Frequency (GHz)	Gain (dB)	NF (dB)	Pdc (mW)	OCP_{1dB} (dBm)
This work	130n BiCMOS	CE & Cascode	75	26	6.4	33.5	+5.5
[46]	350n BiCMOS	CE	77	20	5.8	40	+3
[47]	120n BiCMOS	CE	94	27	8	27.6	-
[48]	250n BiCMOS	Cascode	70	22.5	<7.2	52	+4.5
[48]	130n BiCMOS	Cascode	70	25	<9	54	+1
[49]	130n BiCMOS	CE	80	20	9	63	-

4 Millimeter-Wave Buffer Amplifier

An additional amplifier was needed to provide further gain in the receiver chain as vector modulator in the receiver chain is highly lossy and it is degrading the gain from the low noise amplifier. This additional amplifier is sometimes called as buffer amplifier. The buffer amplifier is placed after the vector modulator.

4.1 Design of Buffer Amplifier

During the design of this buffer amplifier, the main consideration was gain. Noise was not that important design factor because the low noise amplifier has sufficient gain to suppress the noise contribution to significant extent. The schematic of buffer amplifier is shown in Figure 4.1. Due to the simplicity of the design and to have moderate gain, a common-emitter stage was used as buffer amplifier.

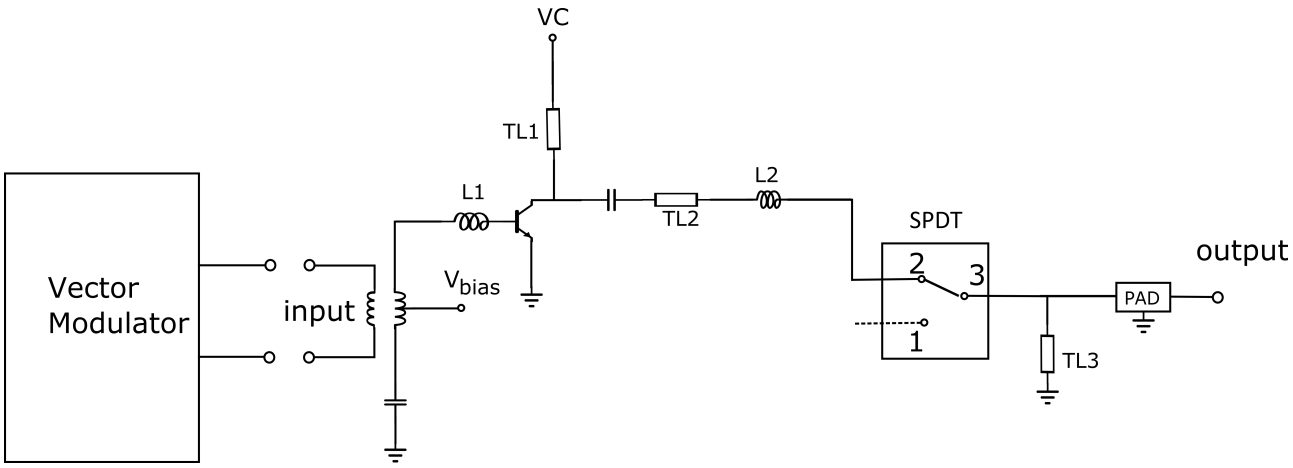


Figure 4.1: Schematic of E-band buffer amplifier

The input of buffer amplifier is connected to the output of the vector modulator. As the output from the vector modulator is differential ended and the input of buffer amplifier is single ended, a transformer balun was used for the differential to single ended conversion. The transformer was designed in similar fashion as in section 3.11.2. The primary of the transformer is connected to the vector modulator whereas the secondary is connected to buffer amplifier. As one terminal of secondary is connected to the ground, to prevent the DC current to flow through the grounded terminal a DC block capacitor is used. The inductor L1 and the transformer was used to match the input of the amplifier.

The output of amplifier is connected to the output port through the switch. The switch is used as the matching element of the buffer amplifier. Transmission line TL1, TL2 and inductor L2 were used to match the output of the amplifier. Although inductor and transmission line moves the similar way on the Smith chart, an inductor was used because it takes smaller silicon area. Transmission line TL3 was used to

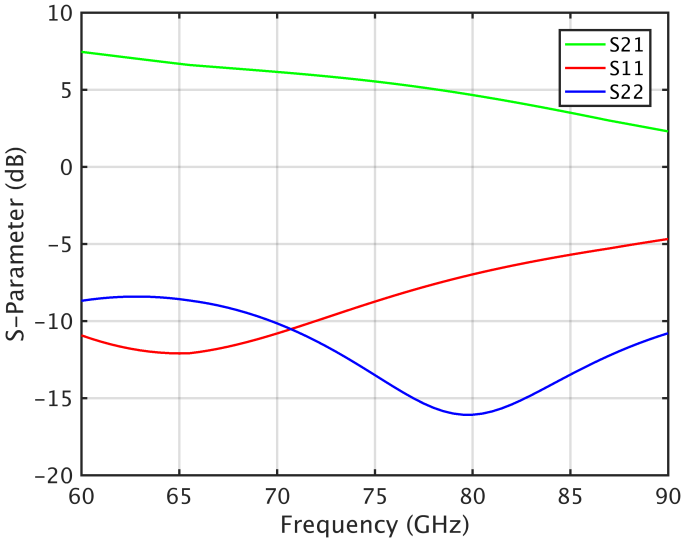


Figure 4.2: Simulated s-parameters of of E-band buffer amplifier

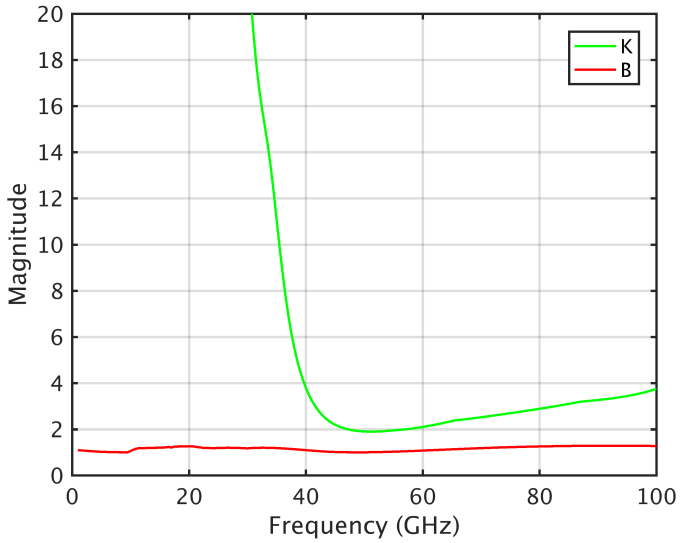


Figure 4.3: Simulated stability factor (K) and stability measure (B) of E-band buffer amplifier

resonate out the pad capacitance. The length of transmission line TL3 could be increased to improve the output matching of the receiver path further. However, it would affect the transmitting path. Therefore, TL3 has been used to resonate out only the pad capacitance.

4.2 Simulation Results

The simulated s-parameters of the designed E-band amplifier are shown in Figure 4.2. The designed amplifier achieved a gain of around 6 dB at 75 GHz. Simulation result shows an wideband output matching of better than 10 dB from 70 to 90 GHz. Input matching is 8.5 dB at 75 GHz. The gain of the amplifier could be increased by increasing the current consumption but this gain was sufficient to achieve the goal.

Figure 4.3 shows the simulated stability factor (K) and stability measure (B) from 0 to 100 GHZ. The value of K is greater than 1 and the value of B is greater than 0 for all the frequencies which represent that the amplifier is unconditionally stable within the frequency range. The DC current consumption is 7.2 mA from the 1.2 V supply which is 8.6 mW.

5 Receiver Performance Analysis

After designing the low noise amplifier, switch, vector modulator and buffer amplifier separately they are integrated together as shown in Figure 5.1. The performance from the post layout simulation of the receiver chain from port 1 to port 2 is shown and analyzed in this section.

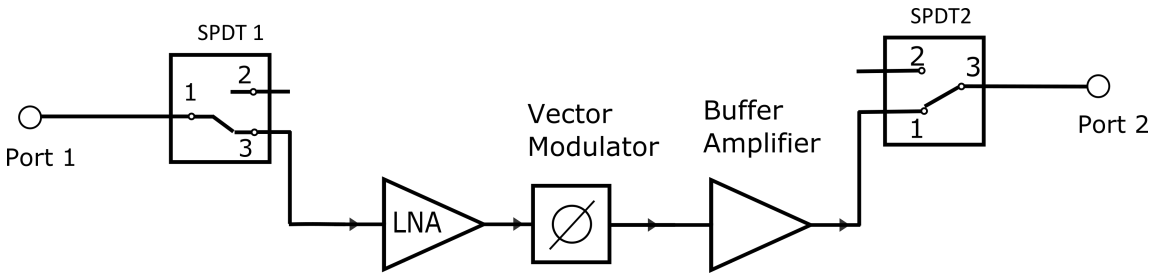


Figure 5.1: Block diagram of the E-band receiver path

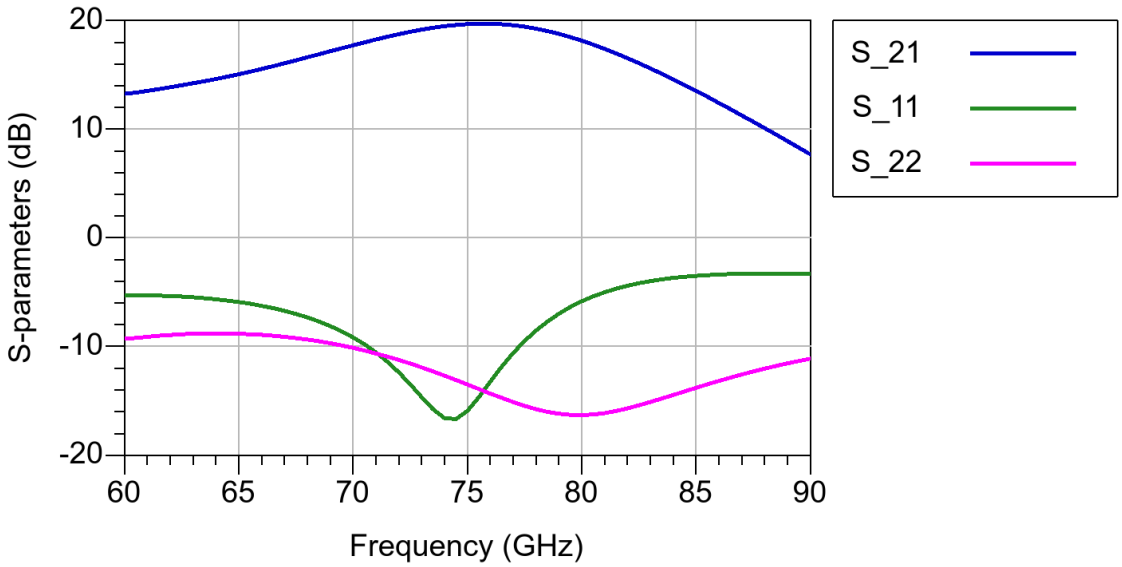


Figure 5.2: Simulated s-parameters of the E-band Receiver

Figure 5.2 shows the simulated s-parameters for the designed E-band receiver. The receiver achieved a gain of 19.6 dB. The 3 dB bandwidth is 12 GHz from 78 GHz to 82 GHz. Input matching is 14 dB at 75 GHz and better than 10 dB from 70 GHz to 77 GHz. The output matching is better than 9 dB from 60 GHz to 90 GHz. The noise figure of the receiver path is shown in figure 5.3. The receiver achieved a noise figure of 6.9 dB at 75 GHz and less than 8 dB within the 3 dB bandwidth from 68 to 82 GHz. Figure 5.4 shows the simulated output 1 dB compression point of the receiver. The achieved P_{1dB} is -5.9 dBm.

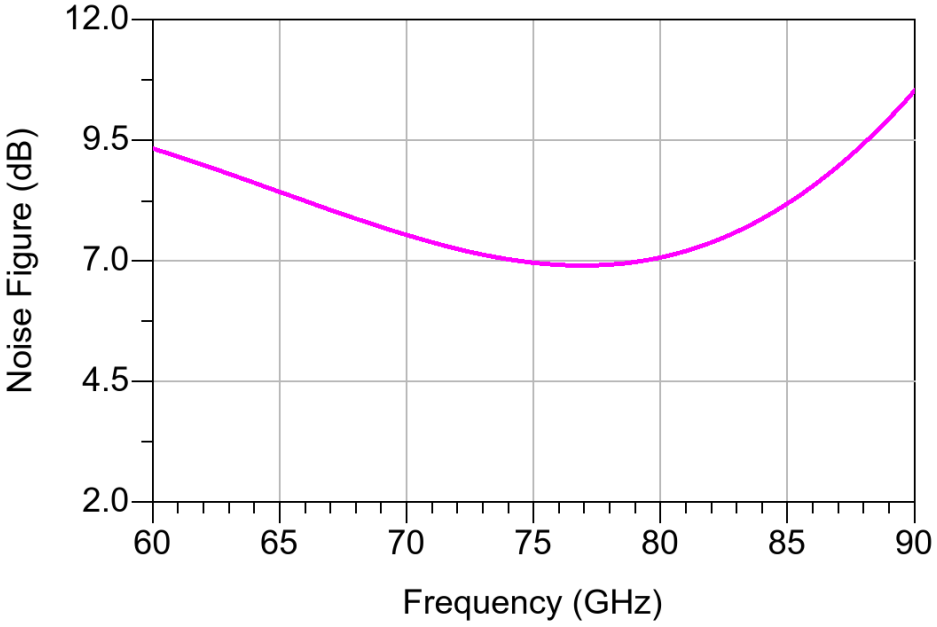


Figure 5.3: Simulated noise figure of the E-band Receiver

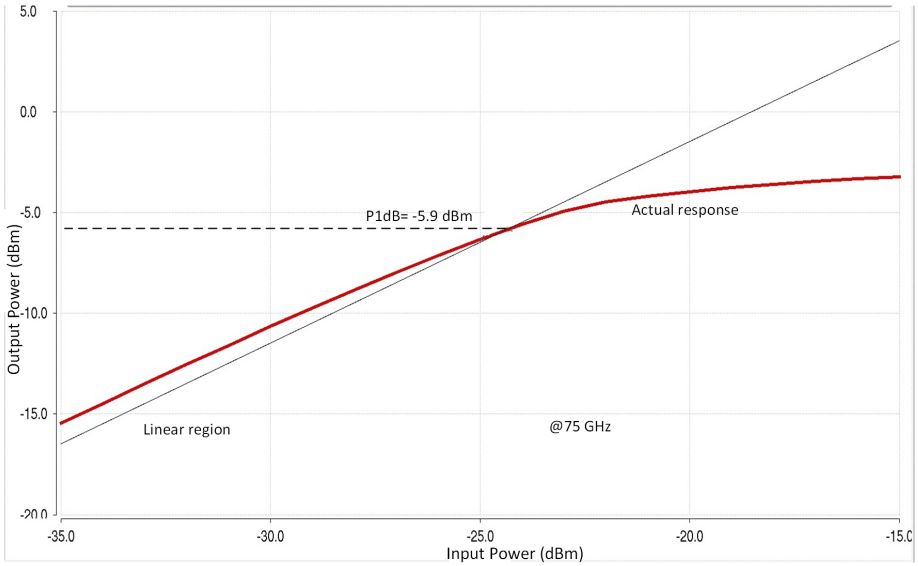


Figure 5.4: Simulated noise figure of the E-band Receiver

Power consumption of each element in the receiver path is shown in Table 5. When both of the switch is turned on the total power consumption is 28 mW. However, the average power consumption is 14 mW. The power consumption of the complete receiver is 103.14 mW.

The final layout of the E-band receiver is shown in the Figure 5.5. The layout area is

Table 5: DC Power consumption of each element in the receiver

Element	Power Consumption (mW)
Switch	14
LNA	33.5
Vector Modulator	47
Buffer Amplifier	8.64
Total	103.14

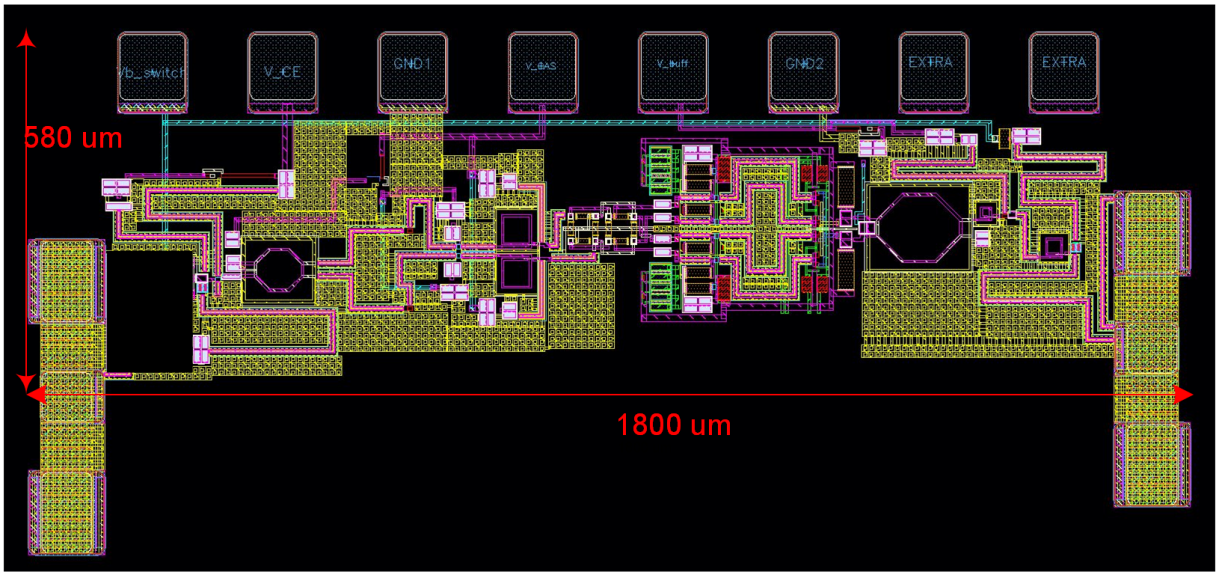


Figure 5.5: Final layout of the E-band Receiver

(1800um)(580um)= $1.044mm^2$ for the receiver. The bottom blank area will be used for the transmitter part. The first element is switch that is covered by a black box in the left side due to confidentiality. The next element is the low noise amplifier. To reduce the layout area, meander type structure of the transmission line was used. The connection between low noise amplifier and vector modulator was made in such a way that the vector modulator remains symmetric as the symmetry plays an important role in the phase of vector modulator. Similarly, buffer amplifier was connected to vector modulator.

6 Conclusion

This thesis has presented the design and analysis of millimeter-wave radio front-end circuits for the fifth generation(5G) wireless communication in a 0.13um silicon-germanium(SiGe) BiCMOS process. The designed radio front-end circuits were single-pole double-through (SPDT) switch, low noise amplifier (LNA) and buffer amplifier(BA) as a part of radio frequency(RF) transceiver system for E-band.

The millimeter-wave single-pole double-through (SPDT) switch has been designed utilizing both the forward and reverse saturated SiGe heterojunction bipolar transistor(HBTs). The performance of both forward and reverse saturated quarter-wave shunt switch topologies has been analyzed. A significantly low loss and high isolation has been achieved with both of the topologies. However, the switch with reverse saturated HBTs offers better insertion loss performance than it's counterpart. Therefore, the quarter-wave shunt switch with reverse saturated HBTs has been chosen for implementation. The resulting reverse saturated switch shows an insertion loss of 1 dB , isolation of 26 dB, reflection coefficient better than 25 dB at 75 GHz and provides a bandwidth of 40 GHz.

Some important considerations related to design of millimeter-wave low noise amplifier such as stability, noise figure, gain and nonlinearity have been discussed theoretically. A two stage millimeter-wave low noise amplifier has been designed. The common-emitter has been chosen at the first stage due to the lowest noise figure whereas a differential cascode amplifier has been used at the second stage due to the highest possible gain. Simultaneous noise and impedance matching is used in order to realize both low noise and high gain. The transformer balun has been used to convert single ended to differential ended signal. Post layout simulation results have been analyzed. The LNA has achieved a peak gain of 26 dB at 75 GHz and a 3 dB bandwidth of 12 GHz from 68.7 GHz to 82.7 GHz. The achieved noise figure is 6.4 dB at 75 GHz and less than 7 dB from 67 GHz to 86 GHz. The LNA consumes DC power of 33.5 mW. The stability has been analyzed in various ways including the stability factor, stability measure, load and source stability circles. The LNA has been found to be unconditionally stable in all methods.

An additional buffer amplifier has been designed to provide sufficient gain in the receiver chain. In the design of buffer amplifier, the main concentration has been paid to the gain . The buffer amplifier has achieved a gain of 5.5 dB at 75 GHz and unconditional stability has been checked in the same manner as in the low noise amplifier design. The amplifier consumes 8.6 mW of DC power.

Finally, the performance of the whole receiver path has been analyzed from the post layout simulation results. The receiver has achieved a gain of 19.6 dB, noise figure(NF) of 6.9 dB and input impedance matching better than 13.5 dB at 75 GHz and output matching is better than 9 dB from 60 to 90 GHz. A 3 dB bandwidth of 12 GHz and 1 dB compression point of -5.9 dBm has been achieved from the designed receiver. The receiver consumes a total DC power of 103.14 mW including

the power consumed by the vector modulator. The total layout area of the receiver is $1.044mm^2$. To reduce the layout area, meandered transmission line has been used. In conclusion, the designed E-band receiver has successfully achieved all the specified requirements.

This thesis focused on design of millimeter-wave receiver for 5G communication. However, the ultimate goal of this work is to develop a complete millimeter-wave transceiver system. For this complete transceiver system, focuses will be on several other design aspects. The power handling of millimeter-wave single-pole double-through (SPDT) switch will be analyzed further to improve the power handling capability. The final receiver has been sent for fabrication. The receiver will be measured and analyzed to verify it's functionalities after fabrication. The transmitter will be designed, fabricated and measured in the next run. After that the transmitter, receiver and mixers will be integrated together to complete the design. Finally, whole transceiver will be fabricated and measured to justify the desired functionalities.

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